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THERMAL RESISTANCES OF JOINT ARMY NAVY (JAN) CERTIFIED MICROCIRCUIT PACKAGES

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The actual thermal resistance value of Joint Army Navy (JAN) certified microcircuit packages was determined. The thermal resistance from the junction to the case (θ_{jc}) was used to characterize the JAN packages. A thermal chip with uniform heating was used for the thermal testing. The thermal chip eliminates much of the ambiguity of thermal testing and is the recommended method for thermal characterization of packages. Thermal resistance values were obtained from over 2,000 tests on various integrated circuit packages assembled and provided by 20 manufacturers. The majority of the tests were performed using .060 inch by .060 inch thermal test chips, simulating small scale integration, attached with a gold silicon eutectic. Selected tests using larger die, simulating medium and large scale integration, and silver glass die attachment were also performed. The thermal resistance data has been tabulated and is reported by type of package construction.

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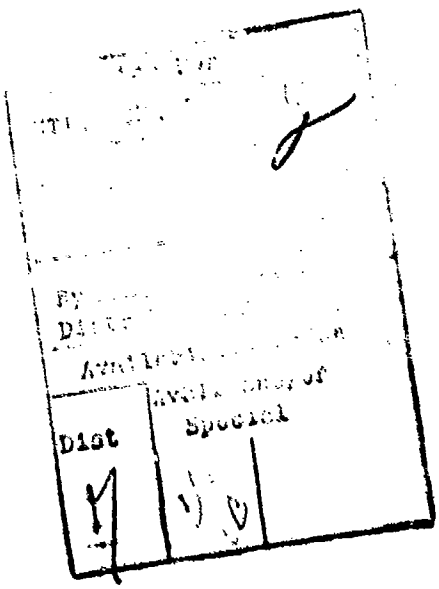

SUMMARY

This report summarizes the activities of Contract F30602-84-C-0067 entitled "Thermal Resistance of JAN Packages".

The reliability of integrated circuits is a complex function of the type of circuit, manufacturing and screening history, the number of interconnects, operating parameters, speed and temperature of operation. In general, reliability will depend upon the activation energy of individual failure mechanisms and the junction temperature. The ability to predict, measure and assure proper junction temperatures is essential to guaranteeing integrated circuit reliability and performance.

Thermal resistance values are used to predict integrated circuit temperatures. The thermal resistance value defines the temperature differences that exist between a device junction on an integrated circuit chip and a specified reference point when a given amount of power is applied to the chip. A low thermal resistance number means that for a given amount of power, the integrated circuit junctions will operate at lower temperatures, which should provide a longer mean time between failures. Significant variations exist in the methods and techniques used to thermally characterize integrated circuits. Reported thermal resistance values vary from less than 10°C/watt to as high as 200°C/watt depending upon the manufacturer, the package type and test technique. Estimates of system reliability are meaningless without more appropriate values for thermal resistance of the integrated circuit packages.

The objective of this contract was to determine the actual thermal resistance value of Joint Army Navy (JAN) certified microcircuit packages. The thermal resistance from the junction to the case (θ_{jc}) was used to characterize the JAN packages. This thermal resistance was selected because it represents the primary heat flow path for hermetic devices.

A thermal chip with uniform [illegible] was selected for the thermal testing. The thermal chip eliminates much of the ambiguity of thermal testing and is the recommended method for thermal characterization of packages. The thermal chip has a structure whereby adequate power can be provided for a large temperature difference between the reference point and the integrated circuit junction for accurate measurements. It has separate sensor and heater elements for real time direct temperature measurements and it has a suitable design whereby the sensor appropriately estimates average junction temperatures.

The thermal resistance was measured by heating the thermal chip junction to 100°C while maintaining the device case on a heat sink at 80°C. The temperature of the case at the heat sink was measured. The thermal resistance was then calculated by subtracting the case temperature from the junction temperature and dividing by the power supplied to the thermal chip.

Thermal resistance values were obtained from over 2,000 tests on various integrated circuit packages assembled and provided by 20 manufacturers. The majority of the tests were performed using .060 inch by .060 inch thermal test chips, simulating small scale integration, attached with a gold silicon eutectic. Selected tests using larger die, simulating medium and large scale integration, and silver glass die attachment were also performed.

The thermal resistance data has been tabulated and is reported by type of package construction. It was found that thermal resistance values varied by more than ± 20 percent from different manufacturers for the same package construction. These variations were due in part to design differences as well as variations in the die attachment process. In general, these variations were more significant for a given type of package construction than were variations in the number of leads. For this reason, packages of the same construction but with a different number of leads are grouped together.

Analysis shows that die attach is a significant thermal problem even for the .060 inch by .060 inch die. The data indicates that approximately 50 percent of the ceramic dual inline packages (the most popular integrated circuit package) have incomplete die attachment. Increases in thermal resistance of approximately 50 percent to 75 percent were seen for small chips with incomplete die attach. Increases of over 300 percent were seen for large chips with incomplete die attach. Although die fillet inspections prior to seal are a requirement for JAN devices, thermal resistance and x-ray data indicates that the sealing process performed after inspection is significantly altering the integrity of the die bond joint.

Further study is recommended to empirically correlate design parameters with thermal resistance values to verify the reasons for incomplete die attach and to investigate techniques for non-destructive die attachment verification. Further analysis is also recommended to determine peak and average junction temperatures that result from non-uniformly heated die.

PREFACE

As the electronics industry pursues faster speeds, greater functional densities and higher reliability, thermal characteristics of microelectronic components become exceedingly more important. There is sincere interest on the part of the integrated circuit industry to provide devices with appropriate thermal resistance values - interest characterized by the high level of participation of various integrated circuit manufacturers in the performance of this contract.

High Technology Sensors would like to acknowledge the outstanding cooperation of the following suppliers who provided samples and other services for evaluation of the thermal resistance of JAN integrated circuit packages.

- Advanced Micro Devices
- Analog
- Fairchild (Mountain View, California)
- Fairchild (Puyallup, Washington)
- Fairchild (South Portland, Maine)
- Harris Corporation
- Intel
- Intersil
- Monolithic Memories
- Mostek
- National Semiconductor
- Precision Monolithics
- Raytheon
- RCA
- Signetics
- Siliconix
- Solid State Scientific
- Texas Instruments
- Zilog
- Chip Supply
- Johnson Matthey
- TRW

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I. INTRODUCTION

The objective of this effort was to determine the actual thermal resistance of Joint Army Navy (JAN) certified microcircuit packages and the effect that die size and die attach material have on thermal resistance.

A number of techniques have been developed over the years for measuring the thermal resistance of integrated circuits. These techniques can be categorized by the method used to estimate the junction temperature. Currently, Method 1012.1 of Military Standard 883 allows the measurement of junction temperature either directly - by viewing the infrared emissions of the junction, or indirectly - by use of a temperature sensitive device parameter on the integrated circuit chip. The measurement by direct viewing requires removing the package lid and coating the chip with a material of a known emissivity. The temperature can then be determined by measuring the radiative power of the source. Although this technique is a direct measurement of junction temperature, it is cumbersome and prohibits package mounting configurations dependent upon the presence of the lid.

No special treatment of the integrated circuit is required for indirect measurements of thermal resistance. Input and output devices already present on the integrated circuit are used to generate the heat and to measure the junction temperatures. However, indirect measurements suffer from an inability to dissipate enough power in the input or output circuits to raise the temperature of the chip sufficiently for an accurate measurement. As integrated circuits become larger and more complex, this is a severe handicap. Additionally, since only input and output devices are used, the indirect technique can not measure the junction temperatures at locations of high power dissipation within an operating circuit. Hence, the temperature measurement does not represent average junction temperatures and may possibly not represent peak junction temperatures achieved on the chip.

Thermal chips offer a number of advantages over direct and indirect measurement techniques. Using appropriate design rules, uniformly heated thermal chips provide an excellent estimate of average junction temperature for an integrated circuit (1). Thermal chips can also be designed to dissipate enough power to raise the junction temperature sufficiently above the reference temperature for accurate and repeatable measurements. The use of thermal chips removes a considerable amount of ambiguity from thermal measurements and increases the accuracy required for the appropriate characterization of integrated circuit packages.

Although thermal chips provide an appropriate measurement of junction temperature, good thermal resistance measurements require that the reference temperature and package mounting techniques be specified. The reference temperature with the most meaning for hermetic devices and the one used for these tests was the bottom of the package underneath the chip. This area is generally the hottest point on the exterior of the package and the most widely accepted reference point.

The choices of mounting configuration, on the other hand, vary considerably. Since package thermal characteristics are affected primarily by conduction and convection, test mounting configurations have been used to simulate these heat removal methods. The simplest configurations use forced air convection or liquid immersing: the sample is surrounded by moving air or a moving liquid. Although these techniques are simple to implement and require no tooling, the measurements do not represent mounting configurations generally used by the military. In another configuration devices are mounted on printed circuit boards and tested in still air. This technique simulates many applications, but, the case and reference temperatures are difficult to control and variations in thermal parameters cause some ambiguity in the test results.

The most repeatable approach is to mount the package on a carefully controlled heat sink. This configuration, outlined in Method 1012.1 of Military Standard 883, was used for these measurements. The heat sink method provides the best control over the reference temperature and this mounting configuration is used on components dissipating high levels of power.

Three types of thermal resistance tests were performed using the heat sink method. The objective of the tests and a brief description are provided in the following paragraphs.

a). Determine the thermal resistance of the JAN certified packages. The JAN certified packages, listed by part number in Appendix A, were tested. Appendix A was generated from a package list provided by the Defense Electronics Supply Center (DESC) as of April, 1984 and from a survey of JAN manufacturers in April, 1984. For these tests, the thermal chip was bonded to the package with AuSi eutectic. For each package, 14 specimens were prepared using .060 inch by .060 inch chips. After assembly over 80 percent of the packages had 10 or more test specimens. The large number of specimens was necessary to assure repeatability of the tests and to obtain statistically viable results for each package. No data was accepted on packages with less than 6 specimens.

b). Show the relationship between chip size and package thermal resistance. A set of packages representing dual inline and hermetic chip carriers was tested to show the effect that chip size has on the thermal resistance. Three chip sizes corresponding to Small Scale Integration (SSI), Medium Scale Integration (MSI), and the Large Scale Integration (LSI) die dimensions were used. For each package tested, a minimum of 20 test specimens were prepared: 10 specimens with the small thermal chip, 10 specimens with the medium thermal chip. If the package cavity was large enough, 10 specimens with the large thermal chip were also tested. Package selection for these tests was based on information obtained from manufacturer's drawings and an April, 1984 survey of the sizes of the microelectronic devices used in the packages.

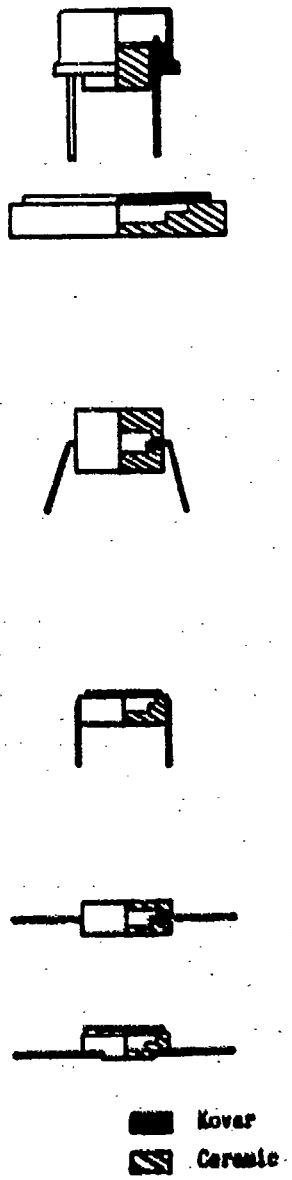
c). Show the relationship between the bonding material and the package thermal resistance. A set of packages representing metal cans, dual inlines, hermetic chip carriers and flat packages was tested to determine the effects of silver glass die attachment. For each package tested a minimum of 20 test specimens were prepared: 10 of the test specimens had silver/glass die attach and 10 had AuSi eutectic die attach. All tests were conducted with .060 inch by .060 inch thermal chips.

Table 1 provides summary information on the thermal resistance of the JAN packages. The thermal resistance data is grouped by the type of package construction. A description of the package construction as well as the mean values and standard deviations are provided.

TABLE 1

SUMMARY DATA

Data Group/ Description	Mean Thermal Resistance (°C/watt)	Standard Deviation (°C/watt)	Reference Figure	Package Construction
I/8 Lead Metal Can	64.20	3.47	10	
II/10 Lead Metal Can	58.64	3.76	10	
III/Chip Carriers (20-68 Terminal)	17.27	1.04	11	
IV/Glass Sealed Dual Inlines with 20 or Less Leads	21.74	2.80	12	
V/Glass Sealed Dual Inlines with 22 or More Leads	21.20	2.21	12	
VI/Side Brazed Dual Inlines with 20 or Less Leads	17.53	2.11	13	
VII/Side Brazed Dual Inlines with 22 or More Leads	16.70	2.09	13	
VIII/Glass Sealed Flat Packages	17.54	2.15	14	
IX/Bottom Braze Flat Packages	16.53	2.30	14	



II. TEST PLAN

A complete test plan was prepared describing the samples to be tested, the test system and the test procedure.

1. TEST SAMPLES

The objective of the program was to determine the actual thermal resistance of the microcircuit packages listed in Appendix A. Each of the packages was measured with .060 inch by .060 inch thermal chips to simulate Small Scale Integrated circuits (SSI). Additional tests using .120 inch by .120 inch thermal chips to simulate Medium Scale Integrated circuits (MSI) and .180 inch by .180 inch thermal chips to simulate Large Scale Integrated circuits (LSI) were performed. Other tests were performed to evaluate Johnson Matthey 4613 die attachment material.

To assist in identifying units for data reduction and for program control, a test cell number was assigned to each part number in Appendix A, for each test using a different die size, and for each test of the silver glass die attachment material. The test cell numbers were composed of two numbers separated by a hyphen. The first number was the High Technology Sensors' package code. This number defined the Case Outline and Configuration of the packages being tested. The second number was a test line number. The 130[1] packages in Appendix A were grouped by package code (Case Outline and Configuration) and were assigned separate test line numbers for evaluation of thermal resistance with .060 inch by .060 inch thermal chips. Eleven packages were also selected for thermal resistance evaluation using .120 inch by .120 inch thermal chips and six packages for evaluation with .180 inch by .180 inch thermal chips. Each package of a given Case Outline and Configuration selected for evaluations with larger thermal chips was assigned an additional test line number for each chip size to be evaluated. Twelve packages were selected for evaluation with silver glass die attachment material using .060 inch by .060 inch thermal chips. These evaluations were also assigned a separate test line number within their respective package codes. Additional test cells were assigned for control samples or tests necessary to assure validity of the measurements. Each test cell contained approximately 10 samples for appropriate statistical evaluation.

Table 2 provides a list of the HTS package codes, their respective Case Outline, and Configuration and generic description of the package. The number of test cells for a given package code are also provided.

1. 117 package types were actually tested.

TABLE 2

TEST CELL DESCRIPTION AND QUANTITY

Package Description				Number Of Test Cells			
HTS Pkg. Code	Case Outline *	Configuration *	Description	.060" x .060" Chips	.120" x .120" Chips	.180" x .180" Chips	JM Material
1	A - 1		8 Lead Metal Can	7	-	-	1
2	A - 2		10 Lead Metal Can	6	-	-	-
3	C - 2		20 Terminal Chip Carrier	1	-	-	-
5	C - 5		44 Terminal Chip Carrier	2	2	1	-
6	C - 7		68 Terminal Chip Carrier	2	1	1	1
7	D - 1	1	14 Lead Dual Inline Pkgs.	12	-	-	-
8	D - 1	3	14 Lead Dual Inline Pkgs.	4	-	-	1
9	D - 2	1	16 Lead Dual Inline Pkgs.	20	1	-	3
10	D - 2	3	16 Lead Dual Inline Pkgs.	8	1	-	1
11	D - 3	1	24 Lead Dual Inline Pkgs.	8	2	1	-
12	D - 3	3	24 Lead Dual Inline Pkgs.	3	1	1	-
13	D - 4	1	8 Lead Dual Inline Pkgs.	6	-	-	-
14	D - 5	1	40 Lead Dual Inline Pkgs.	3	2	1	-
15	D - 5	3	40 Lead Dual Inline Pkgs.	2	1	1	-
16	D - 6	1	18 Lead Dual Inline Pkgs.	6	-	-	-
17	D - 6	3	18 Lead Dual Inline Pkgs.	1	-	-	-
18	D - 7	1	22 Lead Dual Inline Pkgs.	1	-	-	-
19	D - 8	1	20 Lead Dual Inline Pkgs.	5	-	-	-
20	F - 1	1	14 Lead Flat Package	3	-	-	1
21	F - 1	2	14 Lead Flat Package	3	-	-	1
22	F - 2	1	14 Lead Flat Package	4	-	-	1
23	F - 2	2	14 Lead Flat Package	1	-	-	-
24	F - 4	1	10 Lead Flat Package	1	-	-	-
25	F - 4	2	10 Lead Flat Package	1	-	-	-
26	F - 5	1	16 Lead Flat Package	4	-	-	2
27	F - 5	2	16 Lead Flat Package	3	-	-	-
Total:				117	11	6	12

* Per Appendix C of Mil-M-38510

It was desired that the samples be prepared in a manner that best represented the JAN manufacturers assembly techniques. To accomplish this the JAN manufacturers were asked to die attach, bond, inspect for die fillet, seal and hermetically check samples. To control the sample preparation High Technology Sensors provided the thermal chips, an assembly lot traveler, bonding diagrams if desired, Johnson Matthey 4613 material and preforms if desired. In total, over 3,000 thermal chips and 159 bonding diagrams were provided to the IC manufacturers.

Table 3 depicts the sample preparation procedure and the responsibilities assumed by High Technology Sensors and the JAN suppliers. Appendix B is a copy of the assembly traveler and a sample bonding diagram provided by High Technology Sensors. After the samples were received from the manufacturers they were serialized, if required, and kitted into test lots of up to five units for the thermal resistance measurements.

2. TEST SYSTEM

The test system shown in Fig. 1 was used for the measurements. Up to five devices at one time were tested within an air circulating oven. The temperature of the oven was controlled using a platinum resistance sensor and a Barber-Colman 560 series controller. A copper heat sink was installed within the oven. A Precision HDL 5 stabilized liquid bath provided the fluid to the heat sink. Parts were mounted using a silicone thermal grease and positive pressure to copper adapter blocks. The adapter block was then mounted to the heat sink. A metal baffle surrounded the parts under test to reduce convection. Spring loaded thermocouples made contact to the bottom center of the package. A force of approximately 500 grams was applied to this thermocouple to assure appropriate contact. (Poor contact of the package to the heat sink or of the bottom thermocouple to the package could result in inappropriate readings.) Various temperatures were monitored to assure stability including fluid inlet and outlet temperatures, adapter block temperature, air temperature within the baffle and the temperature of the external surface of the baffle.

a). Instrumentation. Instrumentation was configured to minimize measurement errors. Fig. 2 shows the electrical schematic for the thermal test chip power regulation and junction temperature sensing and Fig. 3 the thermocouple readout schematic. Only one device is indicated on these figures for clarity, although five were tested at one time.

TABLE 3

SAMPLE PREPARATION PROCEDURE

High Technology Sensors	Provided Bonding Diagrams Provided Die Attach Material/ Preforms Provided Thermal Chips (14 Per Test Cell) Provided Travelers Provided Instructions and Data Sheets Provided Schedule
JAN Suppliers	Provided Package Samples Provided Drawings on Package Parts Assembled Units . Die Attach . Bond . Die Fillet Inspection . Visual Bond Inspection/No Bond Pull . Seal . Gross/Fine Leak . No Environmental Tests or Burn In . Platting . Bag/Tag or Symbolize

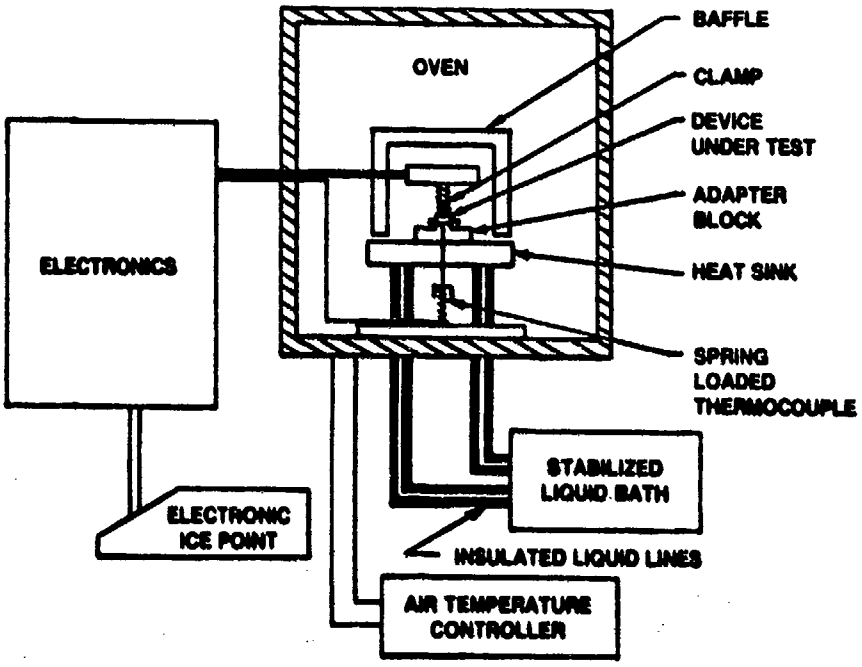


Figure 1. Test System.

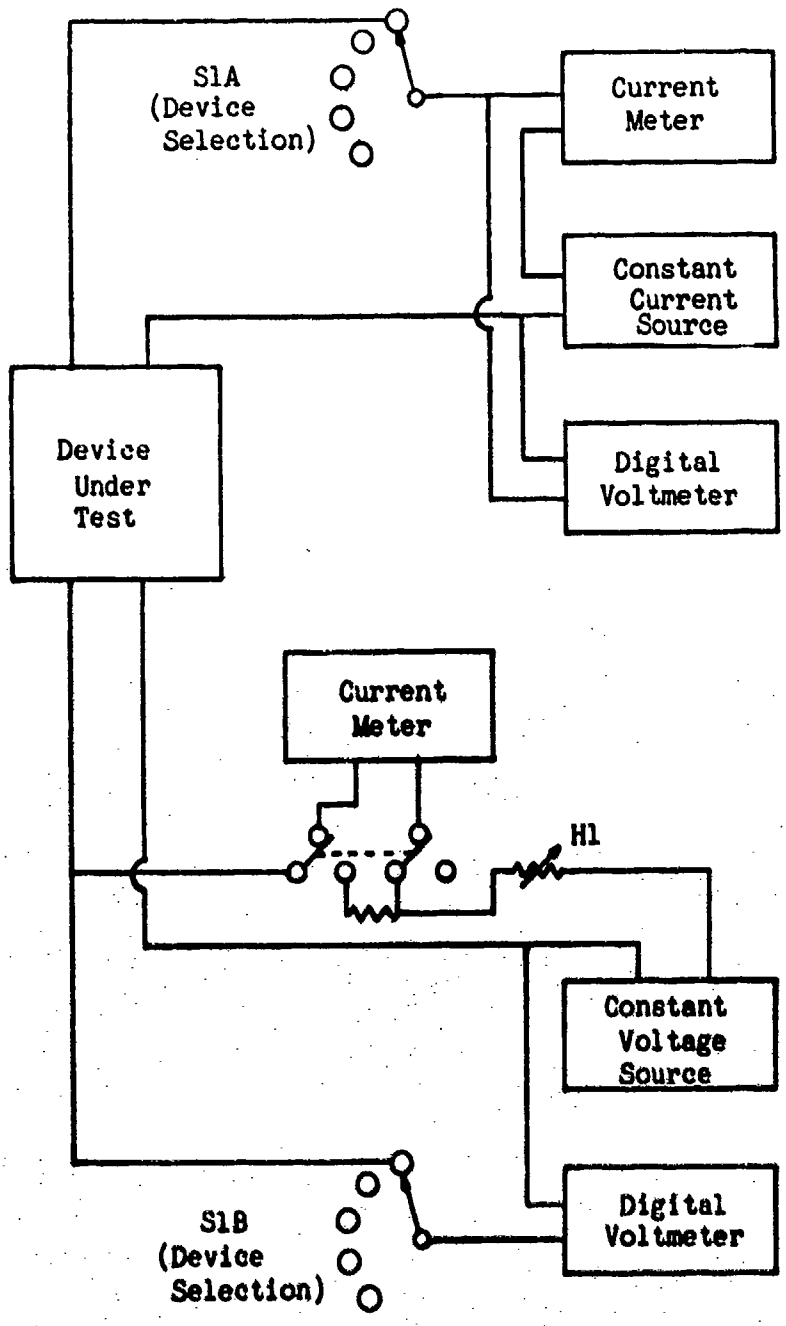


Figure 2. Device Test Schematic.

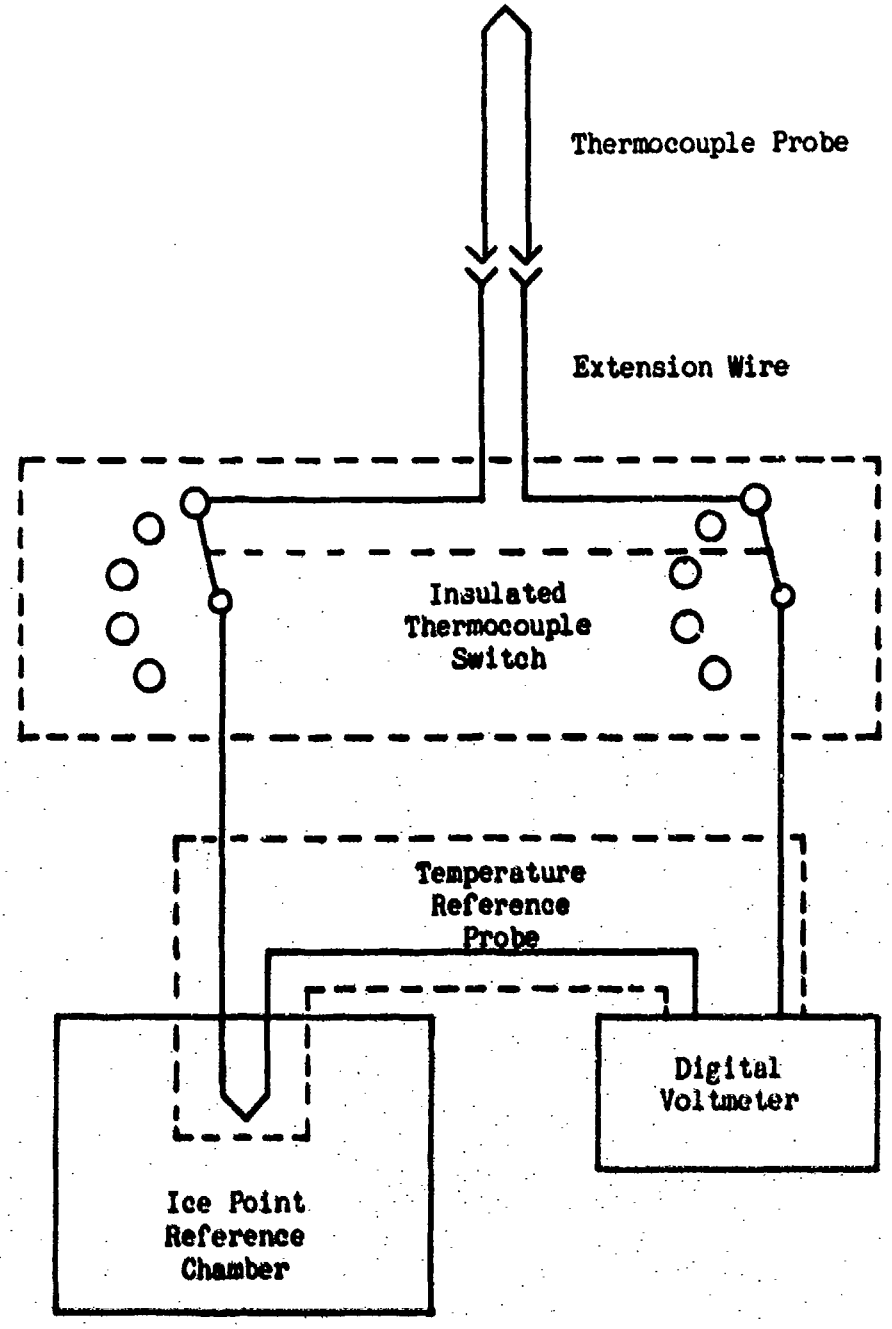


Figure 3. Thermocouple Readout Schematic.

Junction temperature was sensed by applying a constant current to the emitter base junction of the thermal chip and measuring the forward voltage (V_{BE}). Voltage sensing required the use of a digital voltmeter capable of resolving 10 microvolts. Leads between the adapter board and the sensing instruments were selected to minimize induced voltages.

Heating resistors on the test chips were powered to provide a junction temperature of 100°C and a temperature difference between the sensing junction to case of approximately 20°C. The variable resistor H1 was set while monitoring the V_{BE} for each device under test. Individual current adjustment allowed compensation for variations in chip resistors. After stabilization, the actual heater resistor current and heater voltage drop were read for each device. Table 4 lists the equipment used for the testing.

b). Adapter Blocks, Temperature Base and Enclosure. Copper adapter blocks were used to maximize the heat flow from the package under test to the constant temperature base.

Fig. 4 shows the adapter block construction which was used to provide an apparent infinitely variable heat sink path at the bottom of each package base. Thermocouple probe holes were centered under each mounting position to insure accurate measurement of package case temperature (T_C) while minimizing the material removed from the heat sink interface. Mounting holes were provided to fixture the adapter blocks to the liquid regulated base.

A solid copper block (5" x 8" x 1") was used as a liquid-regulated, constant temperature base. The adapter block, with devices, was mounted on the base within the oven. Liquid from a constant temperature bath controlled the temperature of the base.

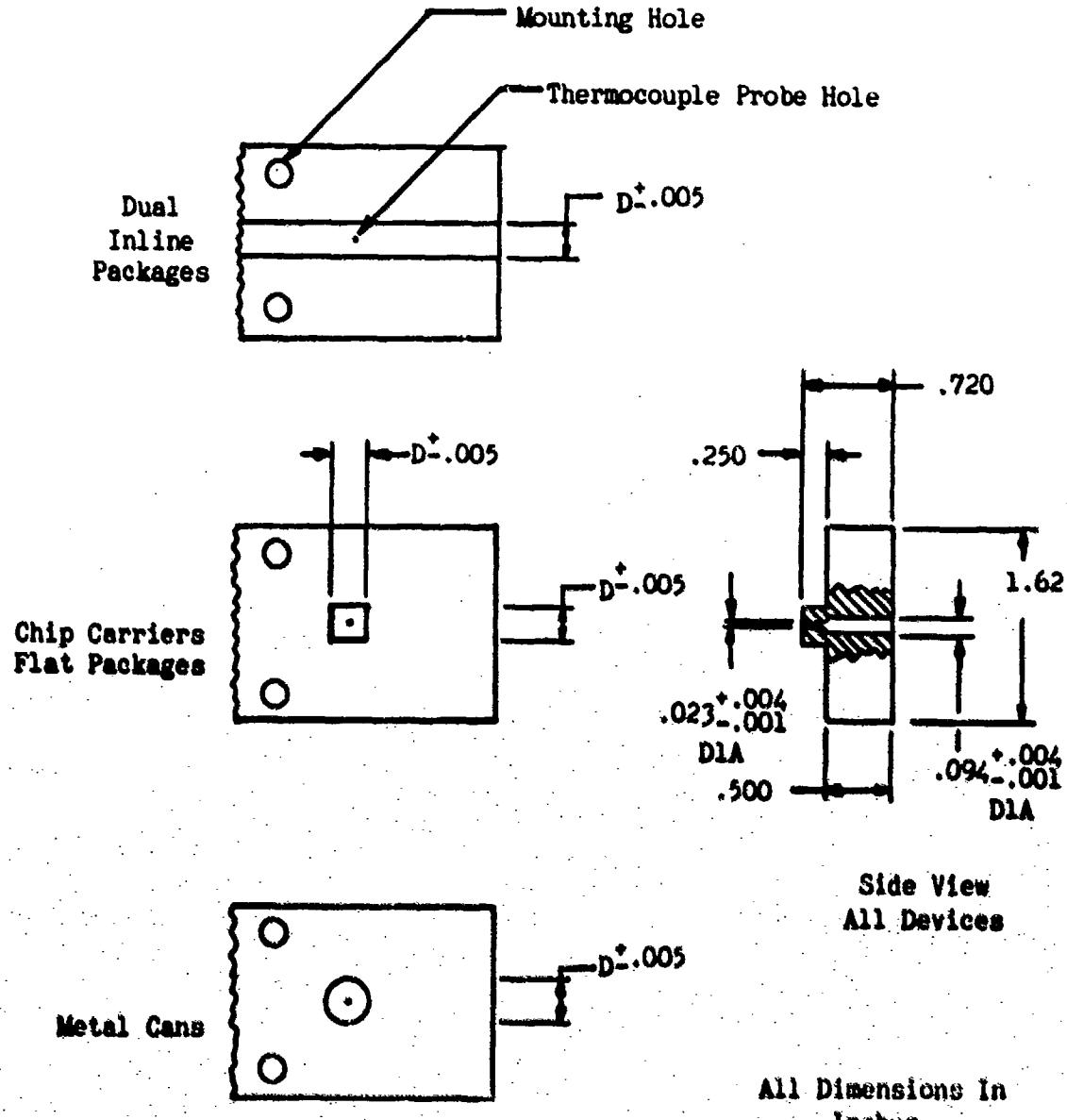
Stabilization of the test set up was accomplished through the use of a baffled temperature chamber or enclosure within the oven.

c). Thermocouples. Type T thermocouples were used based on their accuracy within the temperature range of interest. Grounded shields were used where necessary to minimize extraneous voltage pick up. Subminiature thermocouple probes were used to make contact to the package bottom (Omega type SCPSS-0200-6). The thermocouples were tested at 80°C prior to each test run. Calibration of the thermocouple probes was accomplished using the adapter block and a copper block with a NBS traceable thermocouple located at the package site for transfer calibration. Fig. 5 depicts the calibration structure.

TABLE 4

TEST EQUIPMENT LIST

Sense Element Constant Current Source	Keithly 224
Junction Sensor Digital Voltmeter	Fluke 8810A
Heater Current Meter	HP 3466A
Heater Resistance Power Supply	HP 6206B
Heater Voltage DVM	Fluke 8810A
Thermocouple Digital Voltmeter	Fluke 8810A
Thermocouple Reference Cell	TRC 111 with TRP-T Reference Probe
Temp Controller Circulator Bath	Precision Scientific Model HDL 5
Oven	Blue M Model OV-490A-1
Oven Controller	Barber Colman 560 series



Dual Inline Packages	D = .250, .375, .536
Flat Packages Chip Carriers	D = .230, .505
Metal Cans	D = .160

Figure 4. Adapter Block Construction.

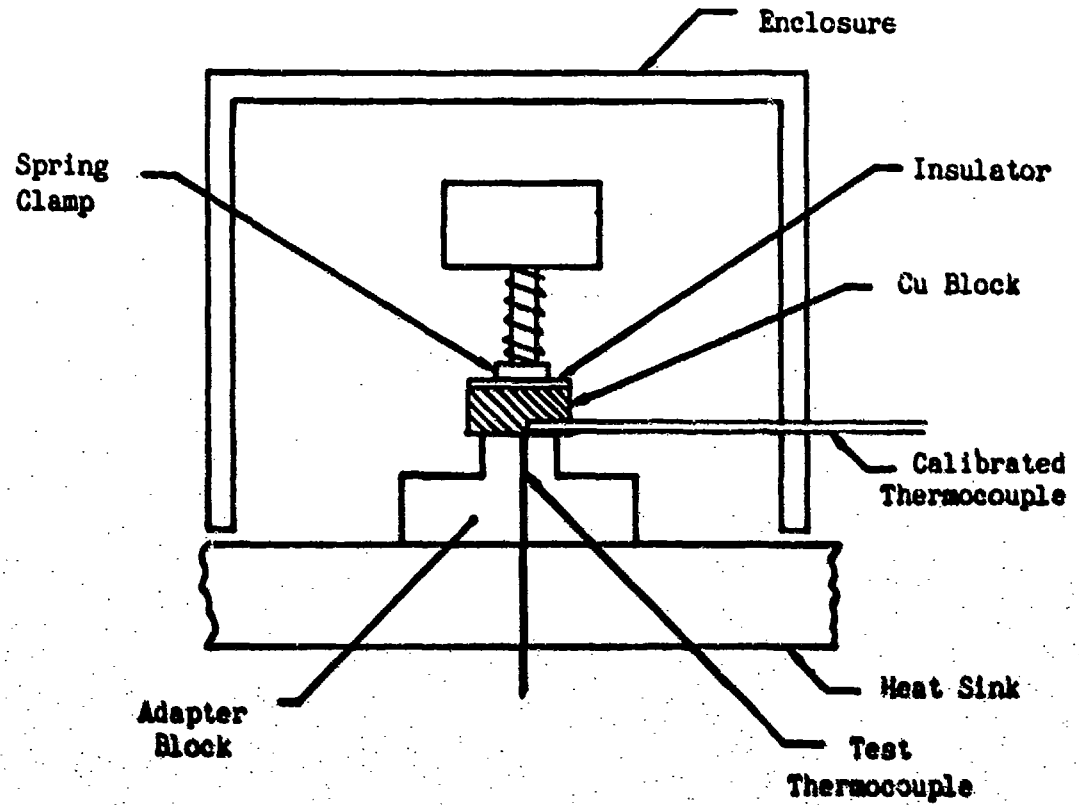


Figure 5. Thermocouple Calibration Structure.

Various thermocouples were used to monitor temperature during test. These monitors are listed below:

Thermocouples 1 - 5	Case Temperature of Device Under Test.
Thermocouple 6	Inlet Temperature of Liquid to Base.
Thermocouple 7	Outlet Temperature of Liquid to Base.
Thermocouple 8	Air Temperature Within Enclosure Above Devices.
Thermocouple 9	Air Temperature Within Enclosure Adjacent to Center Device.
Thermocouple 10	Top of Enclosure.
Thermocouple 11	Temperature of Liquid in Regulated Bath.
Thermocouple 12	Adapter Block.

Additionally, the temperature of the oven and the forward voltage of one of the devices under test were monitored to assure stability.

3. TEST PROCEDURE

To simulate anticipated applications, the thermal resistance measurements were performed in general accordance with Mil-Std 883B Method 1012.1 with modifications to allow greater accuracy in the junction temperature range which has the greatest impact on device reliability. The measurements were performed within an 80°C ambient environment with the junction temperature elevated to 100°C to provide approximately a 20°C difference between the junction and case.

After kitting into test lots, leads were soldered to the devices in order to provide the necessary connections to the electronics. The sensor diode forward voltage and heater resistance were then measured to assure continuity and appropriate wiring. The units were mounted to the adapter block, and then secured to the heat sink within the oven. The enclosure was attached and the continuity was rechecked. Units were then elevated to 100°C for calibration of the sensor junction. After a 12 point stability check, the sensor junction forward voltage was measured at 100°C with 1 ma of current. The temperature of the units was then lowered to 80°C, and a 12 point stability check was performed. The thermal measurements were performed at 80°C by adjusting the current and voltage of the heater until the forward voltage of the sensor junction was within $\pm$ .00004 volts of that obtained at 100°C. Values of the forward voltage within $\pm$ .00001 volts were normally obtained. After stabilization, the temperature of the bottom of the case and the voltage and current to the thermal chip heater were

measured. For each test lot the first unit measured was remeasured to assure that no variations occurred during testing.

To assure uniform testing, a detailed test traveler and data log was maintained. A copy of the traveler is provided in Appendix C.

4. THERMAL CHIP

A Texas Instruments (T.I.) thermal chip was used for the testing (5). The device consisted of four diffused resistors which uniformly covered the chip surface. These resistors are designated R 1, R 2, R 3 and R 4 and had a nominal resistance of 45 ohms. All tests were performed with uniformly heated die obtained by dissipating an equal amount of power in the four resistors. Two transistors, one in the center of the chip (Q 1), and one on the edge (Q 2), were available for temperature sensing. The forward voltage (V_{BE}) of the emitter base junction of the center device (Q 1) at a current of 1 ma was used to determine junction temperature. This measurement was performed with the collector and base shorted together. Chips of .060 inch by .060 inch, .120 inch by .120 inch and .180 inch by .180 inch were available.

Fig. 6 illustrates the T. I. thermal chip layout. The chip layout allowed access to each of the diffused resistors at the points indicated schematically in Fig. 6 as A, B, C, D, E. Fig. 7 provides a schematic of the bias arrangement used for the thermal chip.

Considerable data was collected on the characteristics of the thermal chip. During the course of the testing it was determined that .060 inch by .060 inch devices with a forward voltage (V_{BE}) greater than .600 volts at 100°C gave erroneous results. This conclusion was reached based upon the data shown in Fig. 8, a scatter diagram of the deviation from test lot or test cell mean as a function of V_{BE}. Below a V_{BE} of .601 volts, the thermal resistance values are approximately equally distributed about 0. Above .601 volts the thermal resistance values are skewed to a higher value. Data on units with a V_{BE} greater than or equal to .600 volts were removed from the results. Units with V_{BE} less than .590 volts were generally non-functioning units containing opens or shorts.

Units with low heater breakdown voltages ($<30V$ at 100 uA) also gave erroneous results and were removed from the results. The breakdown was measured between the heater leads and the sensor collector terminal.

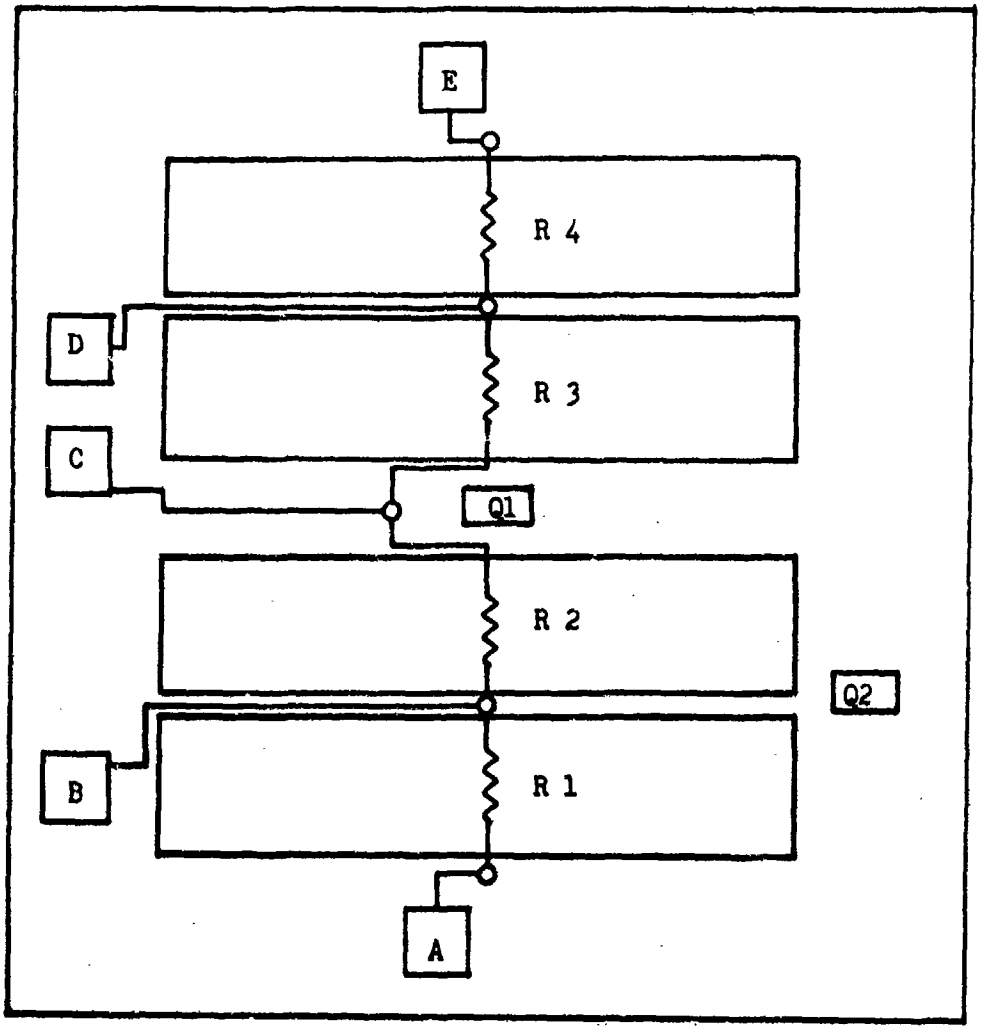


Figure 6. Thermal Chip Layout

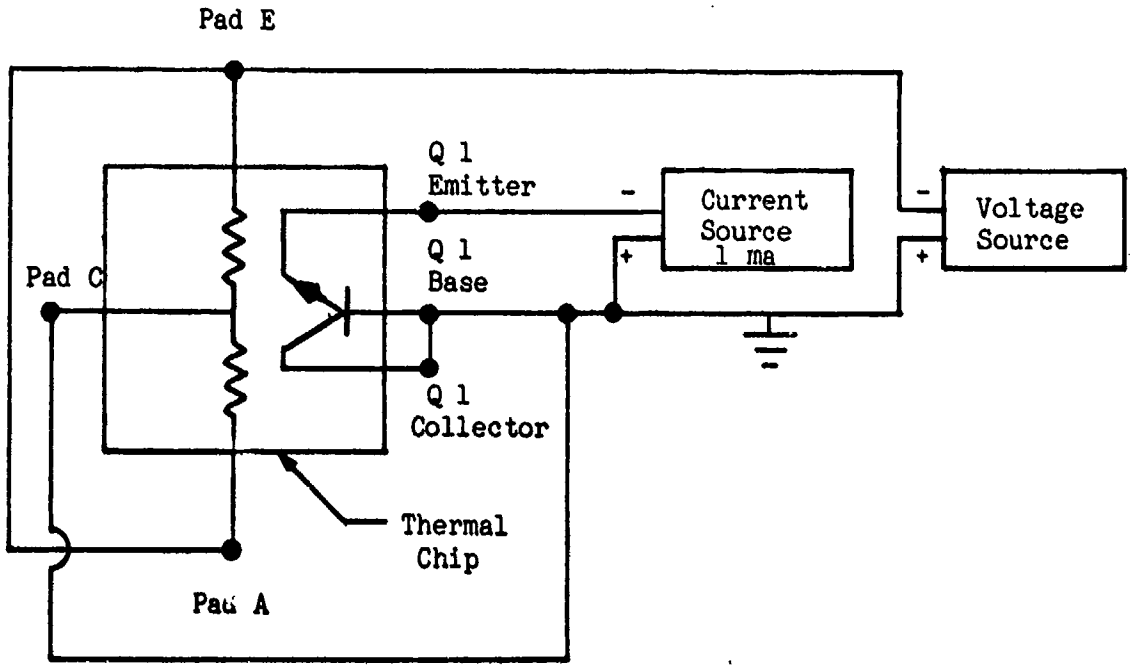


Figure 7. Thermal Chip Bias Schematic.

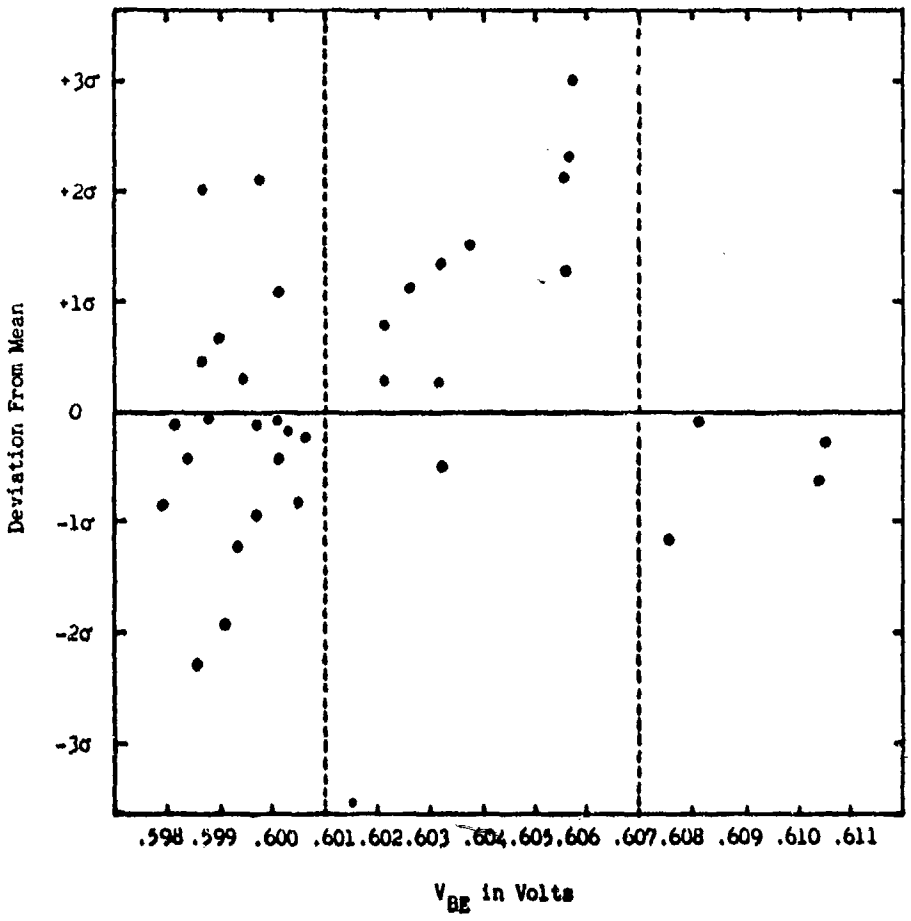


Figure 8. Deviation of Thermal Resistance From Mean vs Forward Voltage (V_{BE})

NOTE: These samples account for only the V_{BE} measured between .598 and .611. The majority of devices had a V_{BE} between .590 and .598. Only 15 out of 732 samples were discarded because of this criteria.

5. TEST SAMPLE STATISTICAL ANALYSIS

Statistics were used for a comparison of results. Samples were retested if they had a thermal resistance value that varied significantly from other thermal resistance values within the same test. Units that then appeared anomalous were analyzed, including data evaluation as well as evaluation by x-ray, visual and electrical tests of the thermal chip. Data was removed from the tests if analysis indicated a test error or a defective sample.

After analysis, the thermal resistance data was collected and ordered from the smallest to largest thermal resistance value for each test cell. If a sample was tested more than once, an average value was used as the value for that sample. A cumulative percentage was calculated for presentation on probability paper.

The mean value, standard deviation and median were also calculated. For test cells with an even number of units, the median was defined as the average of the two middle values. The parameter 2 * sigma/mean (2 times the standard deviation divided by the mean) was calculated to measure the variation within a test cell.

It was discovered that many of the test cells had skewed distributions. To measure the skewness, the moments about the median were calculated per the following equations:

$$\text{Median Moment} \quad (\text{MM}) = \left(\frac{\sum (x - Md)^2}{N} \right)^{1/2} \quad \text{for all x's}$$

$$\text{Lower Median Moment} \quad (\text{LMM}) = \left(\frac{\sum (x - Md)^2}{N_L} \right)^{1/2} \quad \text{for all x's less than the median}$$

$$\text{Upper Median Moment} \quad (\text{UMM}) = \left(\frac{\sum (x - Md)^2}{N_U} \right)^{1/2} \quad \text{for all x's greater than the median}$$

where:

M_d = Median Thermal Resistance (°C/watt)
x = Thermal Resistance Sample Values (°C/watt) for Test Cell
N = Number of Samples
N_L = Number of Samples Less Than The Median
N_U = Number of Samples Greater Than The Median

The ratio of the upper median moment to the lower median moment (UMM/LMM) was also calculated as a measure of skewness.

The significance of variations in mean values of test cells and data groupings was determined by using the Student's t distribution. The larger the value of the t statistic the more significant the difference in mean values of the test cells. The t statistic was calculated per the following equation.

$$t = \frac{\bar{x}_1 - \bar{x}_2}{\sigma(\bar{x}_1 - \bar{x}_2)}$$

where:

$$\sigma\left(\bar{x}_1 - \bar{x}_2\right) = \sqrt{\frac{n_1 s_1^2 + n_2 s_2^2}{n_1 + n_2 - 2}} \sqrt{\frac{n_1 + n_2}{n_1 * n_2}}$$

and:

n_1 = Number of Test Cell 1 Samples

n_2 = Number of Test Cell 2 Samples

s_1 = Standard Deviation of Test Cell 1 Samples

s_2 = Standard Deviation of Test Cell 2 Samples

$\bar{x}_1$ = Mean Value of Test Cell 1 Samples

$\bar{x}_2$ = Mean Value of Test Cell 2 Samples

III. TEST RESULTS

1. DATA GROUPS

JAN packages are specified by case outline as defined in Appendix C of Mil-M-38510. The case outlines are identified by letter-number combinations. The letter F is used to designate flat packages, the letter D for dual inline packages, the letter C for hermetic chip carriers and the letter A for axial lead devices (metal cans). Numbers have been assigned sequentially within each classification for packages with different numbers of leads or different sizes.

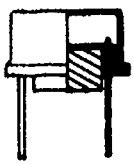
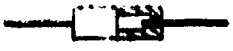
The case outlines have been designed to control the external dimensions of the microcircuit package. Different structures or configurations may be employed by a manufacturer to meet the specified case outlines. These structures are designated by a configuration number for a given case outline. Although the configuration does not significantly affect external dimensions, the construction technique affects internal dimensions, and this has a major impact on thermal characteristics.

Fig. 9 illustrates the package structures and provides the case outlines and configurations tested under this contract. Data for this contract is reported by groupings according to these structures. Analysis indicated that because of the variation that existed from one package to the next, and from one manufacturer to the next for a given structure, further differentiation of data would not be significant and could misrepresent industry values of thermal resistance.

2. TEST DATA

The figures on the following pages contain detailed test data. For each package type, the distribution of all accepted data points is plotted on probability paper. A point (x, y) on the graph indicates that x percent of the units had a thermal resistance of y or less.

To prepare the graphs, all sample data for each package type was ordered from the lowest to the highest value. A percentage was then calculated for each sample. For instance, the data group for dual inline packages with 20 leads or less contained 576 samples, a different percentage was assigned for each of the 576 pieces of data. After assignment of a percentage number for each piece of sample data, the following graphs were prepared by plotting all sample data points, every other, every third or every n^{th} point, depending upon the number of samples within the data group. The mean values, standard deviations and a drawing of the type of package structure are also provided in each figure.

DATA GROUP/ DESCRIPTION	CASE OUTLINE	CONFIGURATION	TYPICAL STRUCTURES
I/8 Lead Metal Can	A-1	Non-Applicable	
II/10 Lead Metal Can	A-2	Non-Applicable	
III/Chip Carriers (20-68 Terminal)	C-2,C-5 C-7	Non-Applicable	
IV/Glass Sealed Dual Inlines With 20 or Less Leads	D-1,D-2 D-4,D-6 D-8	1	
V/Glass Sealed Dual Inlines With 22 or More Leads	D-3,D-5 D-7	1	
VI/Side Brazed Dual Inlines With 20 or Less Leads	D-1,D-2 D-6	3	
VII/Side Brazed Dual Inlines With 22 or More Leads	D-3,D-5	3	
VIII/Glass Sealed Flat Packages	F-1,F-2 F-4,F-5	1	
IX/Bottom Braze Flat Packages	F-1,F-2 F-4,F-5	2	

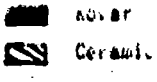


Figure 9. Package Structures

The grid work is identical, and the scale is the same for all figures except the metal cans (Group I and Group II). Comparisons of data by type structure can be made by preparing overlays of the various figures. These graphs can also be used by system designers to analyze the range of thermal resistance values that could be anticipated for a given package structure using chips that correspond to small scale integration. Nominal (mean value), or worst case values of thermal resistance can then be used to develop estimates of the thermal characteristics expected for an electronic system. Finally, device manufacturers can determine how the thermal resistance of their package compares with others in industry.

The data for each package type is composed of a number of test cells with each test cell representing a different package. Data was taken on a minimum of six samples for each test cell. Statistics on the individual test cells are provided in Appendix D. The Appendix data allows further analysis of the variability that exists in thermal resistance values from package to package and manufacturer to manufacturer.

3. DIE ATTACHMENT EVALUATION

The interface between the die and the package has a significant influence over thermal resistance values. JAN manufacturers use gold silicon eutectic for die attachment. This process is difficult to control, is subject to voiding and may induce mechanical stress on the integrated circuit chip. Alternate non-organic die attachment techniques for improved performance and lower costs are sought for military systems. The tests in this section evaluate the effects of silver glass die attachment material on thermal resistance.

A Johnson Matthey die attach paste (JMI 4613) was used for the evaluation. The material consists of four parts silver to one part glass in an organic media. The organic portion consists of a solvent and a depolymerizing resin. The solvent evaporates below 200°C and the resin completely burns off at temperatures below 300°C. Proper use of the material does require a solvent drying cycle and an organic burn out cycle prior to device sealing.

Data from 13 packages of different types was obtained. One hundred thirty nine samples were prepared with Johnson Matthey material. Equivalent test cells prepared with AuSi eutectic had a total of 159 samples. All samples were prepared with .060 inch by .060 inch die. The JAN supplier who prepared the gold silicon samples also prepared the JMI 4613 material samples using identical packages. Table 5 provides the comparison of mean values to thermal resistance obtained for each package for the gold silicon eutectic die attachment and for

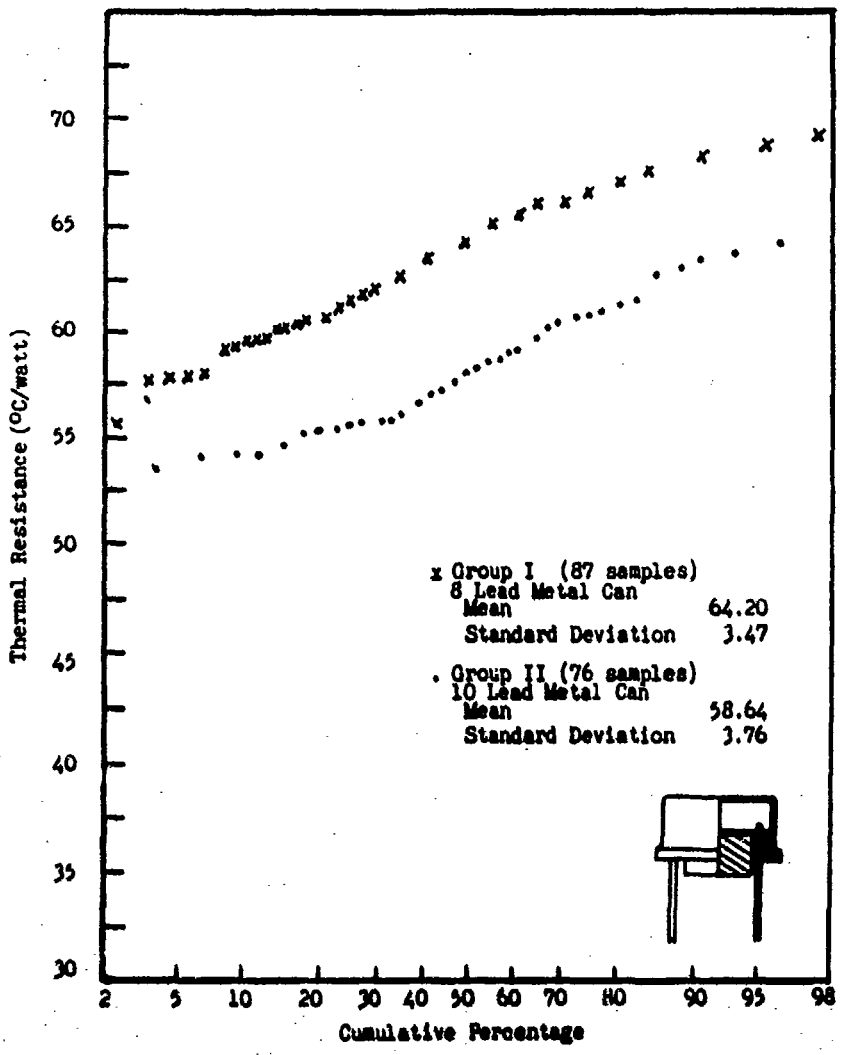


Figure 10. Group I and Group II Thermal Resistance Distributions

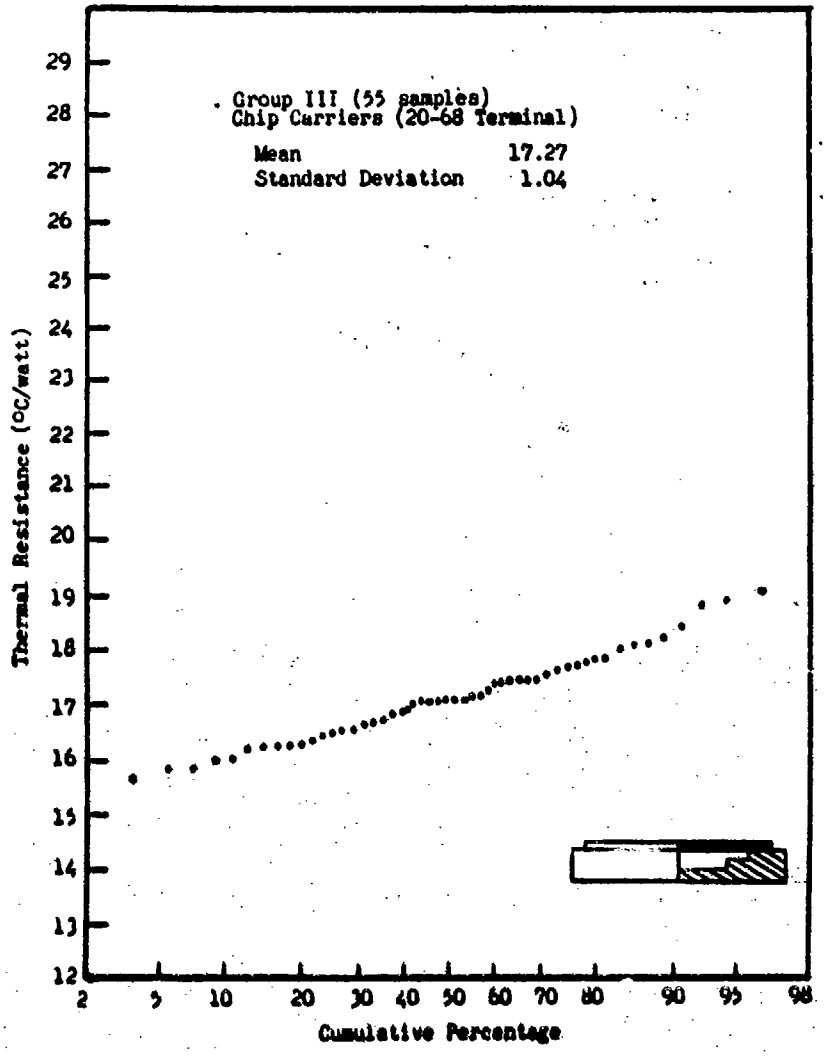


Figure 11. Group III - Thermal Resistance Distribution

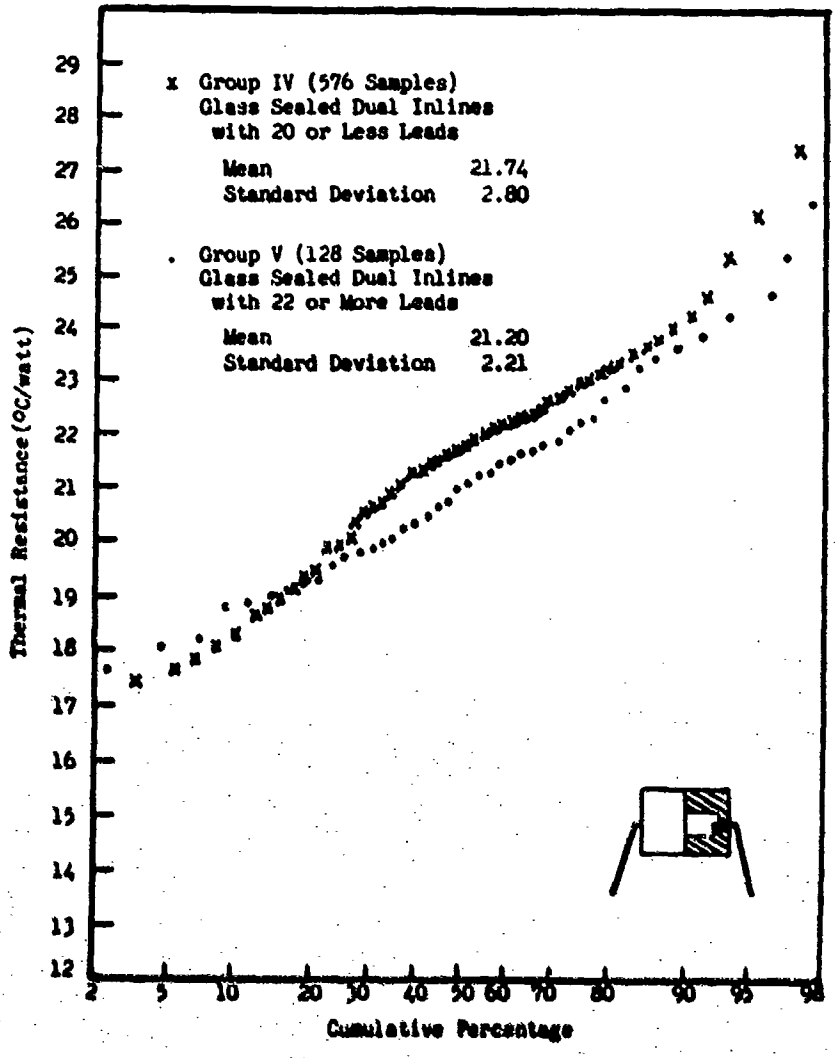


Figure 12. Group IV and Group V Thermal Resistance Distributions

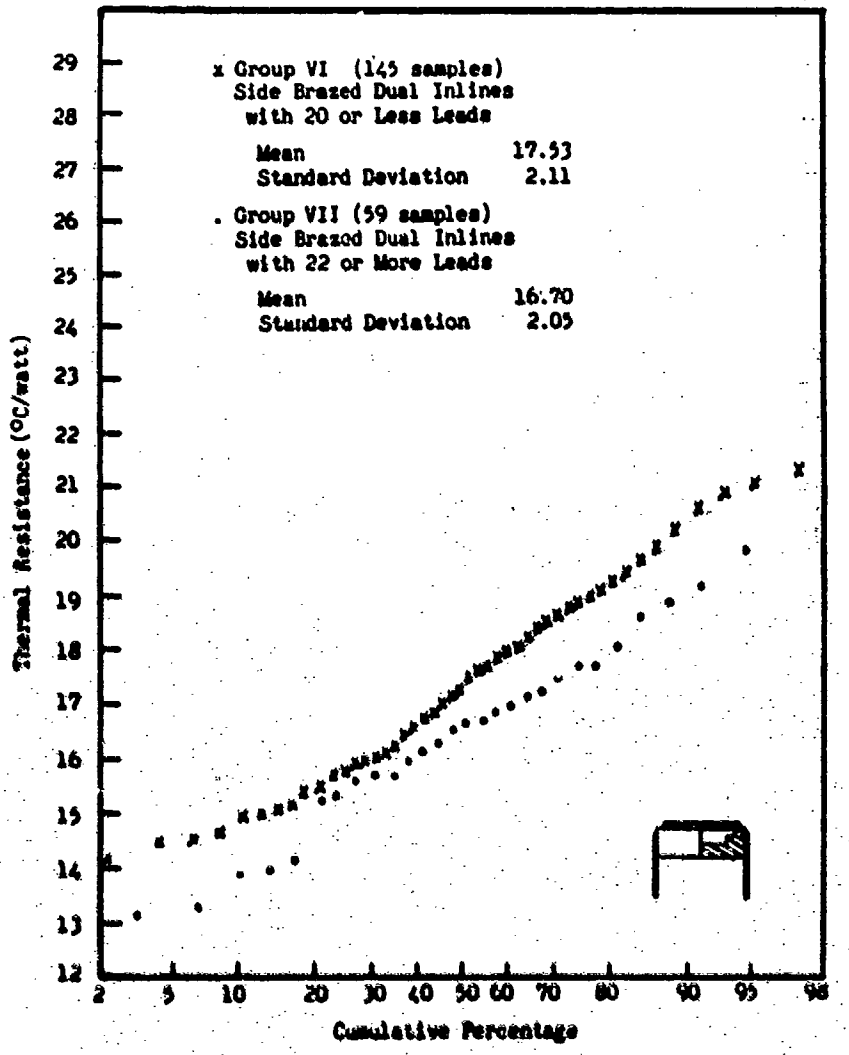


Figure 13. Group VI and Group VII Thermal Resistance Distributions

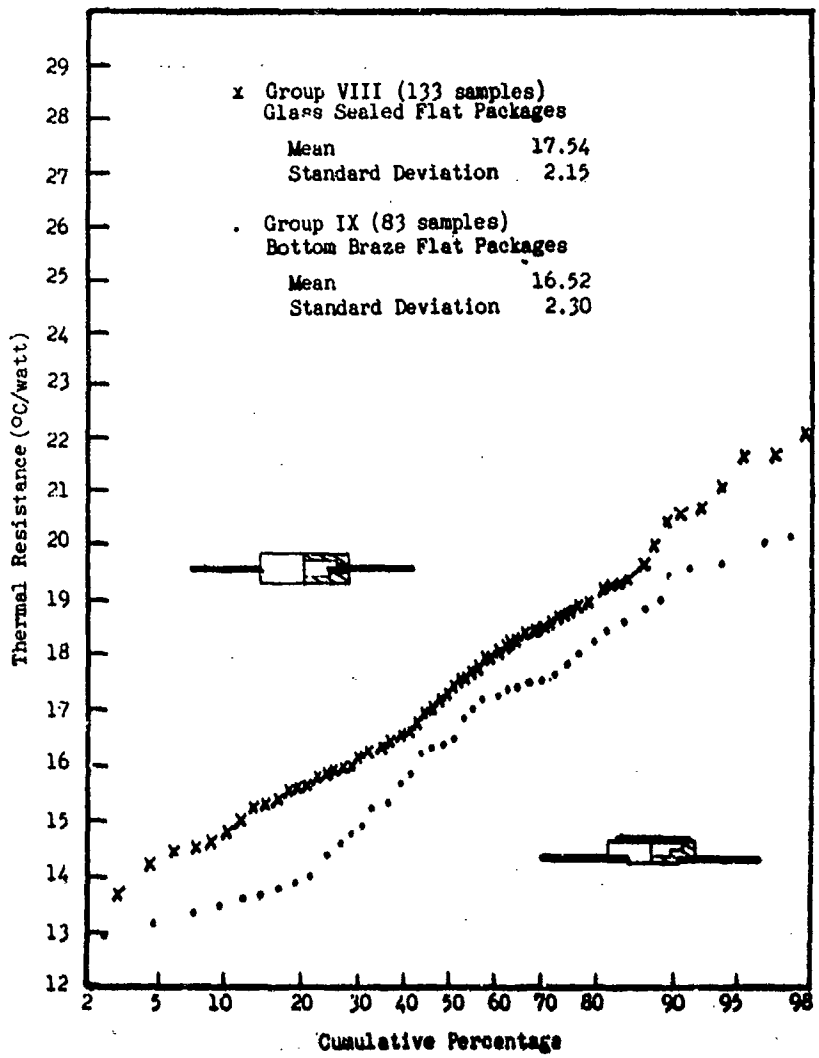


Figure 14. Group VIII and Group IX Thermal Resistance Distributions

TABLE 5

THERMAL RESISTANCE USING JM 4613 AND AU-SI DIE ATTACHMENT

Package Description*	Test Cell Statistic	Gold/Si	JM 4613	t
8 Lead Metal Can (A-1)	Mean (°C/watt)	65.47	61.42	5.63
	Std. Deviation (°C/watt)	2.10	1.45	
	Number of Samples	14	10	
68 Terminal Chip Carrier (C-7)	Mean (°C/watt)	17.69	18.04	1.52
	Std. Deviation (°C/watt)	.577	.341	
	Number of Samples	11	9	
14 Lead Dual Inline Packages (D-1 3)	Mean (°C/watt)	19.05	25.62	11.07
	Std. Deviation (°C/watt)	1.45	1.40	
	Number of Samples	13	12	
16 Lead Dual Inline Packages (D-2 1)	Mean (°C/watt)	22.15	19.85	8.17
	Std. Deviation (°C/watt)	.495	.717	
	Number of Samples	14	7	
16 Lead Dual Inline Packages (D-2 1)	Mean (°C/watt)	21.65	21.38	.61
	Std. Deviation (°C/watt)	.693	1.30	
	Number of Samples	12	13	
16 Lead Dual Inline Packages (D-2 1)	Mean (°C/watt)	18.51	22.45	17.66
	Std. Deviation (°C/watt)	.63	.413	
	Number of Samples	11	13	
16 Lead Dual Inline Packages (D-2 1)	Mean (°C/watt)	21.41	20.84	2.66
	Std. Deviation (°C/watt)	.69	.35	
	Number of Samples	14	14	
16 Lead Dual Inline Packages (D-2 3)	Mean (°C/watt)	19.30	15.61	8.85
	Std. Deviation (°C/watt)	1.16	.89	
	Number of Samples	14	13	
16 Lead Dual Inline Packages (D-2 3)	Mean (°C/watt)	18.85	27.43	12.46
	Std. Deviation (°C/watt)	.685	2.24	
	Number of Samples	13	10	
14 Lead Flat Packages (F-1 1)	Mean (°C/watt)	18.91	16.39	1.78
	Std. Deviation (°C/watt)	3.198	1.999	
	Number of Samples	10	10	
14 Lead Flat Packages (F-1 2)	Mean (°C/watt)	16.63	14.96	3.69
	Std. Deviation (°C/watt)	.96	.99	
	Number of Samples	14	8	
14 Lead Flat Packages (F-2 1)	Mean (°C/watt)	20.02	17.33	3.88
	Std. Deviation (°C/watt)	1.65	1.34	
	Number of Samples	11	10	
16 Lead Flat Packages (F-5 1)	Mean (°C/watt)	14.63	13.67	2.23
	Std. Deviation (°C/watt)	.951	.772	
	Number of Samples	8	10	

* Case Outline and Configuration per Mil-M-38510 Appendix C are shown parenthetically.

Johnson Matthey material. The Student t distribution was used to statistically test the significance of the difference in mean values of the two materials. If the t value shown in Table 5 is higher than 1.73 then the mean values are statistically different with a minimum of 95 percent confidence.

Although the silver glass material has a poorer thermal conductivity than gold silicon, it does not produce as many voids. The data demonstrates that the reduction in the number of voids compensates for the poor thermal conductivity. Further work is recommended to determine if these improvements are seen with larger die size.

Samples from some of the packages with a significantly higher mean value with the JMI 4613 material were provided to Johnson Matthey for evaluation. Their evaluation indicated that the higher thermal resistance values were obtained because of improper glassification or organic burnout.

It should be noted that x-rays were taken of the worst unit from the case outline D-1 configuration 3 package samples prepared with JMI 4613 material. There was no indication of voiding under the die.

It is concluded from the testing that with proper application and process controls, the JMI 4613 material provides thermal resistance values that are better than, or no worse than those obtained for AuSi eutectic. Further work is needed to determine what process controls would be required to assure die attachment with the silver glass material. Current controls have been specifically designed for AuSi die attachment. As an example, the AuSi material does become liquid and does flow. Voids can then be easily detected by x-ray analysis. The x-ray technique does not appear to provide appropriate correlation with poor thermal resistance for the silver glass material. It is suspected that this is because the glass material does not flow as readily as the AuSi material at high temperatures. Other post-seal inspections and/or pre-seal tests for proper glassification may be required.

4. DIE SIZE TESTS

JAN manufacturers assembled integrated circuits with different die sizes within a specific package. The size of the die has a strong influence on the thermal resistance and hence the junction temperatures that will be reached on the integrated circuit. Considerable variability in thermal resistance of a JAN product results not only from variations due to different package structures but also due to die size variations.

The purpose of the die size tests was to empirically determine the relationship between chip size and thermal resistance. The sizes of thermal chips used for the tests were .060 inch by .060 inch, .120 inch by .120 inch and .180 inch by .180 inch. The chips provided were approximate representations of SSI, MSI and LSI die sizes. A set of packages representative of the dual inline packages and hermetic chip carriers was chosen for the tests. Packages were selected based upon maximum chip sizes used by the IC manufacturer.

A total of 11 package types were evaluated. These tests include 3 chip carriers, 5 ceramic dual inlines and 3 side brazed dual inline packages. Data from over 318 units was accepted which included 127 devices with .060 inch by .060 inch chips, 127 devices with .120 inch by .120 inch chips and 64 devices with .180 inch by .180 inch chips. Table 6 summarizes the results.

Fig. 15 shows the distributions obtained for one of the packages. As the figure depicts, the thermal resistance distributions from three different die sizes are plotted on probability paper. The figure illustrates that the distribution deviates from a straight line or normal distribution for a part of the .120 inch by .120 inch chips and for a larger percentage of .180 inch by .180 inch chips. It is hypothesized that this deviation is due to greater voiding of the die bond area. To reduce the complications associated with some samples having reduced die bond areas, the median value of the thermal resistance values for a given die size in a given package was used for analysis. This statistic is more representative of a device with minimal voids.

To show the relationship between die size and thermal resistance, a linear regression of median thermal resistance versus die size was performed per the following equation for each package.

$$\frac{1}{\theta_{jc}} = A_{12} + B_{12} * A_c$$

where:

θ_{jc} = Thermal Resistance From Junction To Case (^{o}C/watt)

A_{12} = Constant

B_{12} = Constant

A_c = Chip Area (inch^2)

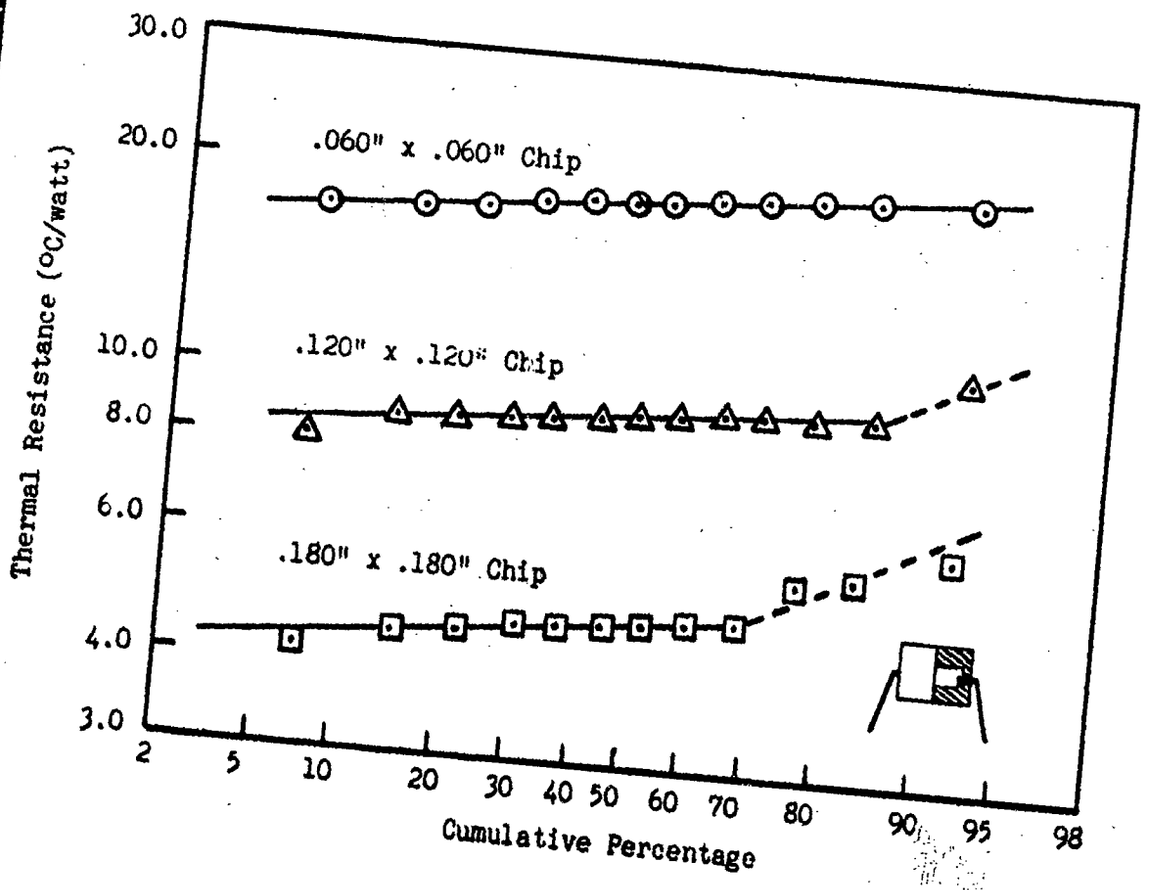


Figure 15. Thermal Resistance For Three Die Sizes For 16 Pin Dual Inline Packages

$$B_{12} = \frac{n \sum x_1 x_2 - (\sum x_1)(\sum x_2)}{n \sum x_2^2 - (\sum x_2)^2}$$

$$A_{12} = \bar{x}_1 - B_{12} \bar{x}_2$$

The constants A_{12} and B_{12} were found for each package. In addition, the statistic $\sigma(B_{12})$ was determined for each package which utilized all three chip sizes. The statistic $\sigma(B_{12})$ is a measure of the error of the estimate of the slope B_{12}. This, in turn, is an estimate of the quality of the relationship between die size and thermal resistance. These statistics are defined by:

$$\sigma(B_{12}) = \frac{\sigma(1.2)}{\sqrt{\sum x_2^2 - \frac{(\sum x_2)^2}{n}}}$$

where:

$$\sigma(1.2) = \sqrt{\frac{\sum x_1^2 - A_{12} \sum x_1 - B_{12} \sum x_1 x_2}{n - 2}}$$

and:

x_1 = Thermal Resistance Sample Median Values

x_2 = Chip Area For Sample Median Values

n = Number of Median Samples = 3

$\bar{x}_1$ = Mean Value of Sample Median Values

$\bar{x}_2$ = Mean Value of Chip Area

Table 6 contains a listing of the A_{12} and B_{12} values as well as $\sigma(B_{12})$. The data indicates that the relationship between the inverse thermal resistance and die area may be effectively modeled for the majority of the devices as a linear relationship with the 1σ error of the estimate of the slope at less than $\pm$ 3 percent. The packages for which $\sigma(B_{12})$ is approximately 10 percent have some anomalies in the thermal resistance distribution which is evidenced by values of 2σ/mean that are greater than .15.

TABLE 6

DIE SIZE THERMAL RESISTANCE VALUES

Type Package	Chip Size	No. Samples	Mean	Median	2σ Mean	Nominal Package Base Thickness	B_{12}	Sigma B_{12}	A_{12}
44 Terminal Chip Carrier (C-5)	.060	10	16.54	16.48	.06	.026	5.995	.0554	.0385
	.120	9	7.98	8.07	.05	.026			
	.180	9	4.35	4.29	.09	.026			
44 Terminal Chip Carrier (C-5)	.060	12	16.86	17.01	.06	.027	4.093	-	.0441
	.120	12	9.67	9.71	.15	.027			
68 Terminal Chip Carrier (C-7)	.060	11	17.69	17.77	.07	.042	5.563	.5639	.0304
	.120	7	9.65	9.89	.15	.042			
	.180	11	4.69	4.67	.10	.042			
16 pin DIP (D-2 1)	.060	12	22.63	22.83	.07	.064	3.745	-	.0303
	.120	12	12.88	11.87	.53	.064			
16 pin DIP (D-2 3)	.060	12	15.64	15.78	.10	.042	6.429	-	.0402
	.120	11	7.54	7.53	.11	.042			
24 pin DIP (D-3 1)	.060	12	20.57	20.62	.13	.058	4.569	-	.0320
	.120	14	10.32	10.22	.08	.058			
24 pin DIP (D-3 1)	.060	11	22.35	22.09	.08	.060	4.554	.0558	.0295
	.120	13	10.36	10.42	.04	.060			
	.180	14	5.67	5.66	.07	.060			
24 pin DIP (D-3 3)	.060	13	18.94	18.96	.10	.040	5.610	.1494	.0310
	.120	14	9.31	9.15	.18	.040			
	.180	12	4.91	4.68	.24	.040			
40 pin DIP (D-5 1)	.060	13	19.78	19.95	.09	.061	4.712	-	.0332
	.120	14	9.89	9.90	.04	.061			
40 pin DIP (D-5 1)	.060	10	19.34	19.17	.07	.059	4.776	.0118	.0351
	.120	11	10.09	9.61	.23	.059			
	.180	8	5.17	5.07	.14	.059			
40 pin DIP (D-5 3)	.060	11	13.77	13.88	.07	.040	4.968	.4315	.0586
	.120	10	7.24	7.28	.11	.040			
	.180	10	4.61	4.31	.43	.040			

Table 6 does show that the inverse thermal resistance of an individual package has a linear relationship with area. The exact value of the slope B_{12} and intercept A_{12} defining that relationship are, however, dependent upon package construction details.

Fig. 16 further illustrates the variation of thermal resistance with die size. The figure provides an average slope and intercept of the inverse thermal resistance for devices with approximately the same ceramic base thickness illustrating the variation in slope and intercept caused by thickness.

The data on the variation in thermal resistance with die size can be used to estimate anticipated thermal resistance values for various die sizes from the thermal resistance data developed for the .060 inch by .060 inch chips. Accurate determinations, however, would require measurements of a particular package with chips of different die sizes.

Further analysis of the data from Table 6 and Fig. 16 shows that as the die size grows larger there is greater variation in thermal resistance values. None of the packages with .060 inch by .060 inch thermal chips had a value of 2σ /mean of .15 or greater for their test cells, however, 8 of 17 of the test cells with larger die had a 2σ /mean of .15 or greater. In one test cell of 12 units the thermal resistance values using a .120 inch by .120 inch thermal chip ranged from a low of 10.28°C/watt to 13.68°C/watt except for one unit which had a value of 23.68°C/watt. X-ray analysis showed that the high thermal resistance value was due to a large amount of voiding under the die.

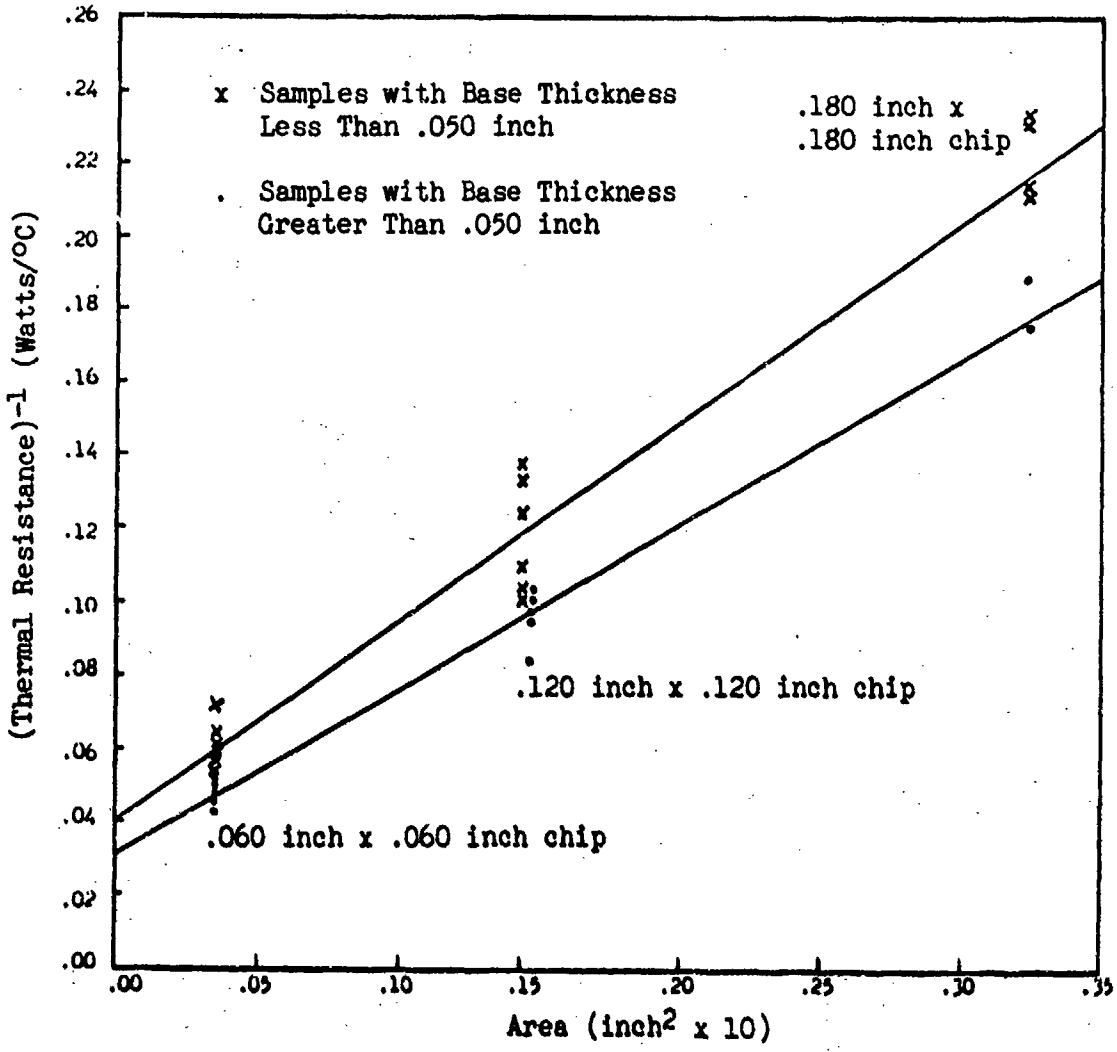


Figure 16. Thermal Resistance vs Die Size

IV. THERMAL RESISTANCE VARIATIONS

In general, the thermal resistance values vary significantly for a given case outline and configuration from manufacturer to manufacturer. These variations are due to two basic factors.

a). The manufacturers have the freedom to select internal physical dimensions and materials. The internal dimensions of the packages are not controlled by military specification. Although package outlines are identical, the package base thickness and cavity depths vary from one manufacturer to the other. Additionally, the thermal conductivity of alumina changes from .03 cal/cm-sec-^{o}C for 90 percent alumina to .045 cal/cm-sec-^{o}C for 95 percent alumina at 100^{o}C. Thus changes in material purity can have additional effects on thermal resistance.

b). Process variations and different process control procedures for parameters effecting die attach exist. The military specifications require 100 percent inspection for die fillet as a pre-seal inspection, however, for glass sealed parts the specifications also require that devices be sealed at a minimum of 385^{o}C, 15^{o}C above the gold silicon eutectic. The sealing temperature may then cause changes to the die bond joint with no requirement for reinspection.

Fig. 17 provides data on three test cells obtained from samples of 16 pin dual inline packages (DIP) packages (Case Outline D-2, Configuration 1 of Mil-M-38510) from three different manufacturers. The thermal resistance variations from manufacturer to manufacturer as shown in Fig. 17 correspond to the differences in ceramic base thicknesses. The nominal base thicknesses by design were 56.6 mils, 67 mils and 71 mils for manufacturers A, B and C respectively. The distribution from manufacturer C is composed of two line segments one of which has a significantly higher slope indicating variations are due to die attachment.

X-ray analysis was performed on units with high thermal resistance variations. The amount of gold under the die and the extent of die fillet, although subjective, did correspond to high thermal resistance values. For further substantiation, statistical analyses were performed. A regression analysis was made on dual inline packages which indicated a linear relationship between the mean value for a test cell and the standard deviation. A histogram of the standard deviation for all test cells for dual inline packages of Configuration 1 is plotted in Fig. 18. As can be seen from the figure this distribution may be described by an exponential distribution. This non-symmetric type of

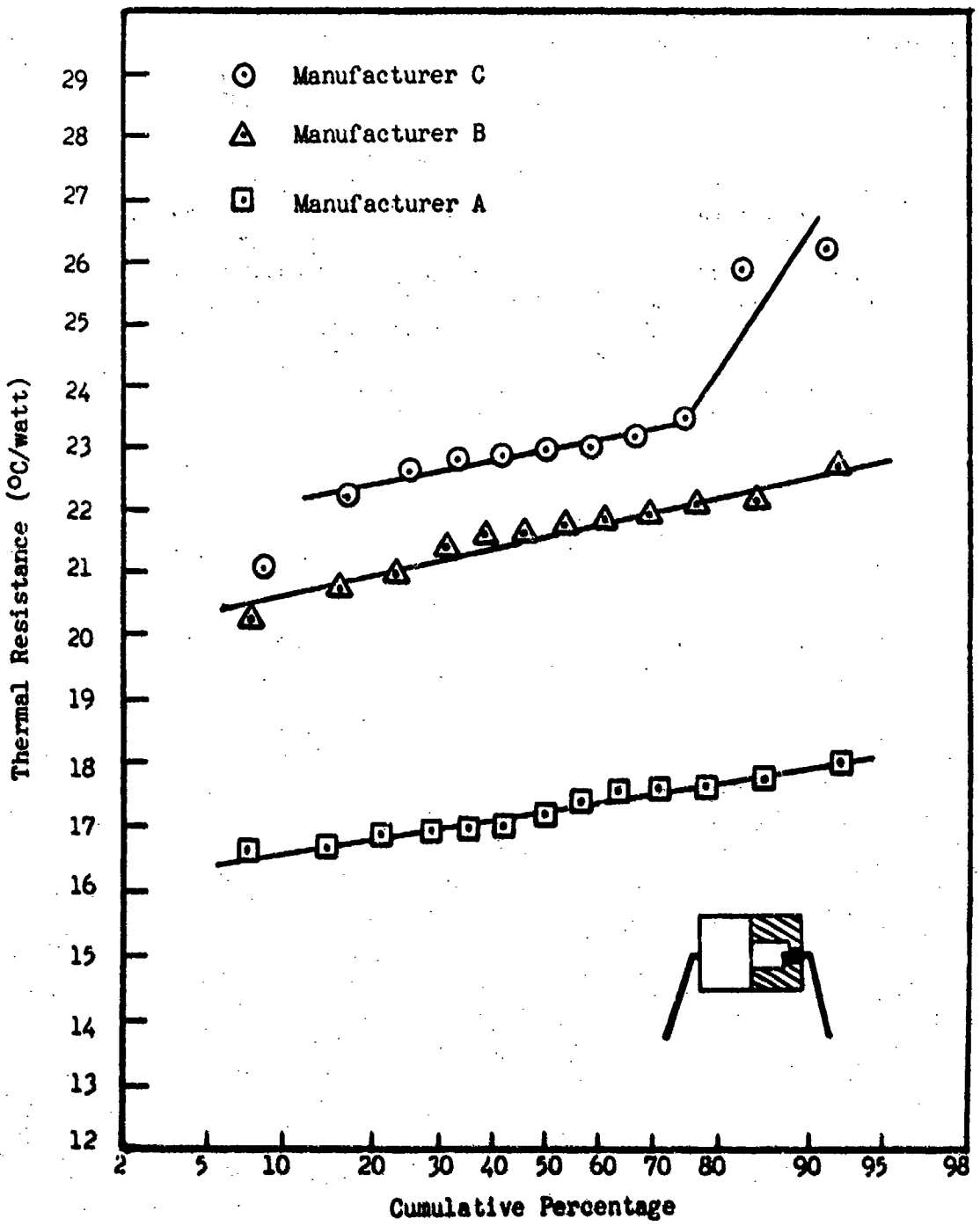


Figure 17. Thermal Resistance of Three Manufacturers For 16 Pin Dual Inline Packages

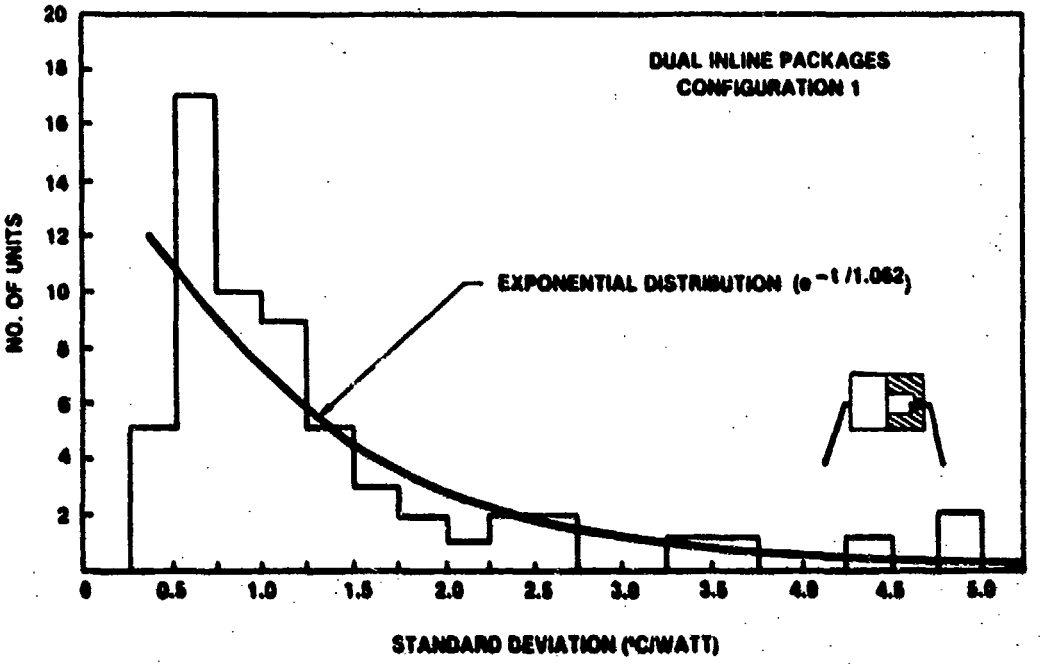


Figure 18. Standard Deviation Histogram For Dual Inline Packages

distribution would be expected from devices having variations in contact area between the die and ceramic base. This indicates that for a given base thickness the thermal resistance variability is controlled primarily by processing conditions.

Fig. 19 illustrates the influence of the above two major factors on thermal resistance. In that figure, data from all of the dual inline ceramic packages of Configuration 1 are plotted on probability paper. The data summarizes over 700 tests from 14 vendors using the .060 inch by .060 inch thermal chip. Below a value of 21.5°C/watt a straight line can be plotted through the data points. This represents a normal distribution. This type variation would be reasonable for variations caused by ceramic base thicknesses due primarily to design variations. Above 21.5°C/watt the shape of the curve differs significantly from a straight line indicating variations caused by incomplete die attachment.

The data from the analysis has been used to define an exponential distribution for the segment above 21.5°C. The data indicates that a minimum of 50 percent of the JAN devices do not have 100 percent die attach between the die and the ceramic base.

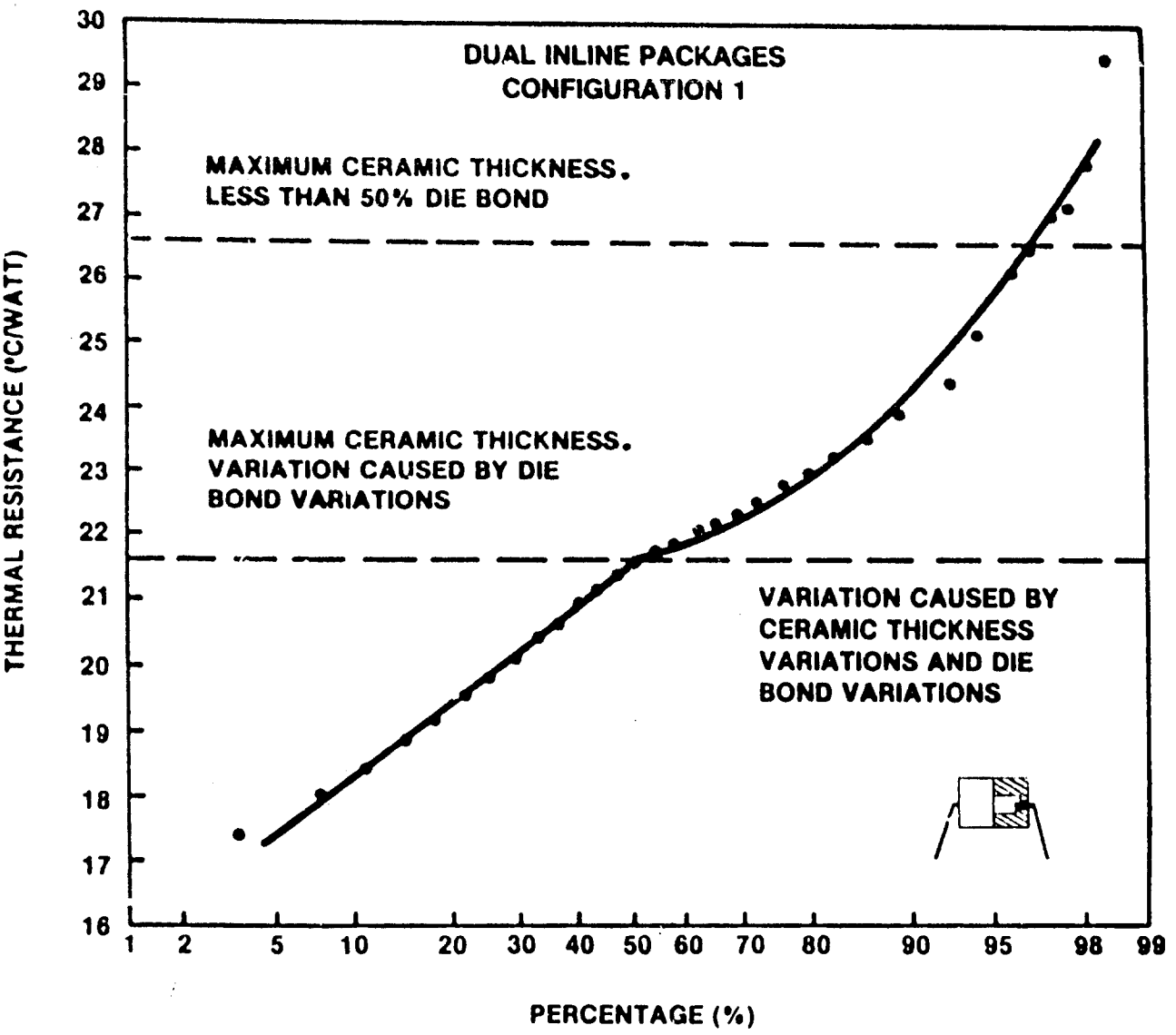


Figure 19. Thermal Resistance of Dual Inline Packages

V. CONCLUSIONS

Much of the ambiguity in thermal resistance measurements of integrated circuit packages disappears when appropriately designed measurements are performed with thermal chips.

Data on the thermal resistance values which can be expected for the JAN integrated circuit packages has been provided. As would be expected, the thermal resistance values for a given die size are determined by the package construction. The variation of thermal resistance values for a given package construction reflects allowable manufacturing design variations and process variations in die bond area.

It has been shown that with appropriate die attachment, the inverse thermal resistance is a linear function of die area for uniformly heated die. Data indicates that as die size increases the ability to obtain controlled die attach decreases.

Furthermore, it has been shown that when Johnson Matthey 4613 die attach material is used in place of the AuSi eutectic that the thermal resistance is not degraded provided appropriate controls are utilized with the material. The data does indicate that when JMI 4613 material is used x-ray analysis will be ineffective in determining a poor joint between the die and ceramic case.

For the first time the extent of the impact of variations in contact area between a silicon die and the ceramic base have been revealed. Analysis indicates that 50 percent or more of the JAN packages of dual inline configuration have voiding to some degree. Further, it is hypothesized that a significant portion of this void is caused by the subsequent high temperature sealing operations.

VI. RECOMMENDATIONS

The activities of this contract have resulted in a number of recommendations and suggestions for improved thermal resistance testing and for further work. These recommendations are listed below.

1. The thermal chips used for thermal measurements need to be well characterized. Appropriate testing needs to be performed to assure a functioning thermal chip and also to assure that thermal chip device parameters do not influence thermal resistance readings. DoD should contract for its own thermal chip design to assure appropriate device design and availability.

2. Standard heat sinks for testing should be employed. Variations from one unit to the next can be altered by different heat sinking techniques.

3. This work provides thermal resistance values for uniformly heated die. Further work is needed to empirically determine peak junction temperatures and thermal resistance values of non-uniformly heated die.

4. Wide variations exist from manufacturer to manufacturer. Further work is recommended to understand the reasons for the wide variations, and the effectiveness of die fillet inspections as a technique for verifying die attachment.

5. Simple techniques for screening the thermal characteristics of die attachment which do not rely on analysis of x-ray radiographs need to be developed.

6. More information is needed on the utilization of Johnson Matthey material for large die sizes.

7. Thermal designers need to consider the lack of complete die attachment in their thermal models. A maximum value of 50 percent die attachment is recommended for analysis.

8. Further work is recommended on larger die sizes to determine if die with die bond areas below 50 percent of the die area are being fielded.

VII. REFERENCES

(1) Oettinger, Frank F., "Thermal Evaluation of VLSI Packages Using Thermal Chips - A Critical Review", Solid State Technology, February, 1984.

(2) Oettinger, Frank F., and Albers, J., "Thermal Test Chips For VLSI Package Evaluations", IEEE VLSI Packaging Workshop, Gaitherburg, MD. September, 1982.

(3) Oettinger, Frank F., Blackburn, David L., Rubin, Sherwin, "Thermal Characterization of Power Transistors", IEEE Transactions on Electron Devices, Vol. ED-23, No. 8, August, 1976.

(4) Baxter, Gene K., Anslow, James W., "High Temperature Characteristics of Microelectronic Packages", Transactions on Parts, Hybrids and Packaging, Vol. PHP-13, No. 4, December, 1977.

(5) Howser, J., Barab, S., Prokop, J., "High Density Low-Cost Microelectronics Packaging Program", AFWAL-TR-82-1077, AD-B069621

APPENDIX A

List of Packages

Manufacturer	Part Number Identification	Case Outline Configuration
Advanced Micro Devices	1-471 (SSI)	D - 1 (1)
	1-459 (SSI)	D - 2 (1)
	1-470	D - 2 (1)
	1-482	D - 3 (1)
	1-467	D - 5 (1)
	2-473	F - 5 (1)
Analog	20100	A - 1
	20130	A - 2
	20240	D - 1 (1)
	20220	D - 3 (3)
Fairchild(Mountain View California)	5B(r)	A - 1
	5F	A - 2
	6A	D - 1 (1)
	7N	D - 1 (3)
	6B	D - 2 (1)
	7B	D - 2 (1)
	7R	D - 3 (3)
	6T	D - 4 (1)
	3I	F - 1 (1)
	3F	F - 4 (1)
	4L	F - 5 (1)
Fairchild(Puyallup Washington)	6D	D - 2 (1)
	7L	D - 3 (1)
	8F	D - 6 (1)
	6S	D - 7 (1)
	3L	F - 5 (1)

APPENDIX A

List of Packages
(continued)

Manufacturer	Part Number Identification	Case Outline Configuration
	4D	S / S
	2I	S / S
Fairchild(South Portland Maine)	6A	D - 1 (1)
	6B	D - 2 (1)
	6N	D - 3 (1)
	4E	D - 8 (1)
	3I	F - 1 (1)
	4L	F - 5 (1)
	3J	F - 2 (1)
Harris	2A	A - 1
	4D	D - 1 (1)
	4Z (MSI)	D - 2 (1)
	4K (LSI)	D - 3 (1)
	4N (LSI)	D - 6 (1)
	5E (LSI)	D - 6 (1)
	1M	S / S
Intel	JD8080	D - 5 (1)
	JD8086	D - 5 (1)
	JD2147/48	D - 6 (1)
Intersil	TW (10-0048)	A - 2
	DD (10-0545)	D - 1 (3)
	DE (10-0150)	D - 2 (3)
	FD (10-0582)	F - 1 (2)

APPENDIX A

List of Packages
(continued)

Manufacturer	Part Number Identification	Case Outline Configuration
Monolithic Memories	16J-1	D - 2 (1)
	16D-1	D - 2 (3)
	18J-3	D - 6 (1)
	18J-5	D - 6 (1)
	20J-1	D - 8 (1)
Mostek	00216-0300	D - 2 (3)
	00216-0500	D - 2 (3)
National Semiconductor	H08C	A - 1
	H10C	A - 2
	J14A (SSI)	D - 1 (1)
	J16A (SSI)	D - 2 (1)
	J16A (MSI)	D - 2 (1)
	J24A (MSI)	D - 3 (1)
	J08A (SSI)	D - 4 (1)
	J20A (LSI)	D - 8 (1)
	F14C	F - 1 (2)
	W14B (MSI)	F - 2 (1)
	F10B	F - 4 (2)
	W16A (MSI)	F - 5 (1)
	F16B	F - 5 (2)
Precision Monolithic	J1	A - 1
	J3	A - 1
	J5	A - 1
	Y2	D - 1 (1)
	Q2 (MSI)	D - 2 (1)

APPENDIX A

List of Packages
(continued)

Manufacturer	Part Number Identification	Case Outline Configuration
	Q3 (SSI)	D - 2 (1)
	Q3 (MSI)	D - 2 (1)
	Q2 (SSI)	D - 2 (1)
	Q1	D - 2 (3)
	Q4	D - 2 (3)
	Z2	D - 4 (1)
	Z3	D - 4 (1)
RCA	DF324E	D - 1 (1)
	AM665A	D - 1 (3)
	DF326E (MSI)	D - 2 (1)
	DF324E	D - 2 (1)
	AM506A	D - 2 (3)
	AM676A	D - 2 (3)
	AM539A (SSI)	F - 2 (2)
	AM467A (MSI)	F - 5 (2)
	AM540A (SSI)	F - 5 (2)
Raytheon	TE	A - 1
	TF	A - 2
	DC	D - 1 (1)
	DM	D - 2 (1)
	MR	D - 3 (3)
	DE	D - 4 (1)
	MQ	D - 6 (3)
	CJ	F - 1 (1)
Signetics	GL	C - 2
	FHC	D - 1 (1)

APPENDIX A

List of Packages
(continued)

Manufacturer	Part Number Identification	Case Outline Configuration
	FHB	D - 1 (1)
	FJC	D - 2 (1)
	FJB	D - 2 (1)
	FJH	D - 2 (1)
	FN	D - 3 (1)
	FNK	D - 3 (1)
	FE	D - 4 (1)
	FKH	D - 6 (1)
	FLH	D - 8 (1)
	WHC	F - 2 (1)
	WHD	F - 2 (1)
	WJC	F - 5 (1)
Siliconix	5450	A - 2
	5419	D - 1 (3)
	5418	D - 2 (3)
	5417	F - 1 (2)
Solid State Scientific	12-0001	D - 1 (1)
	12-0034	D - 1 (3)
	12-0035	D - 2 (1)
	12-0033	D - 2 (3)
Texas Instruments	J14	D - 1 (1)
	J16	D - 2 (1)
	J20	D - 8 (1)
	JT24	D - 3 (1)

APPENDIX A

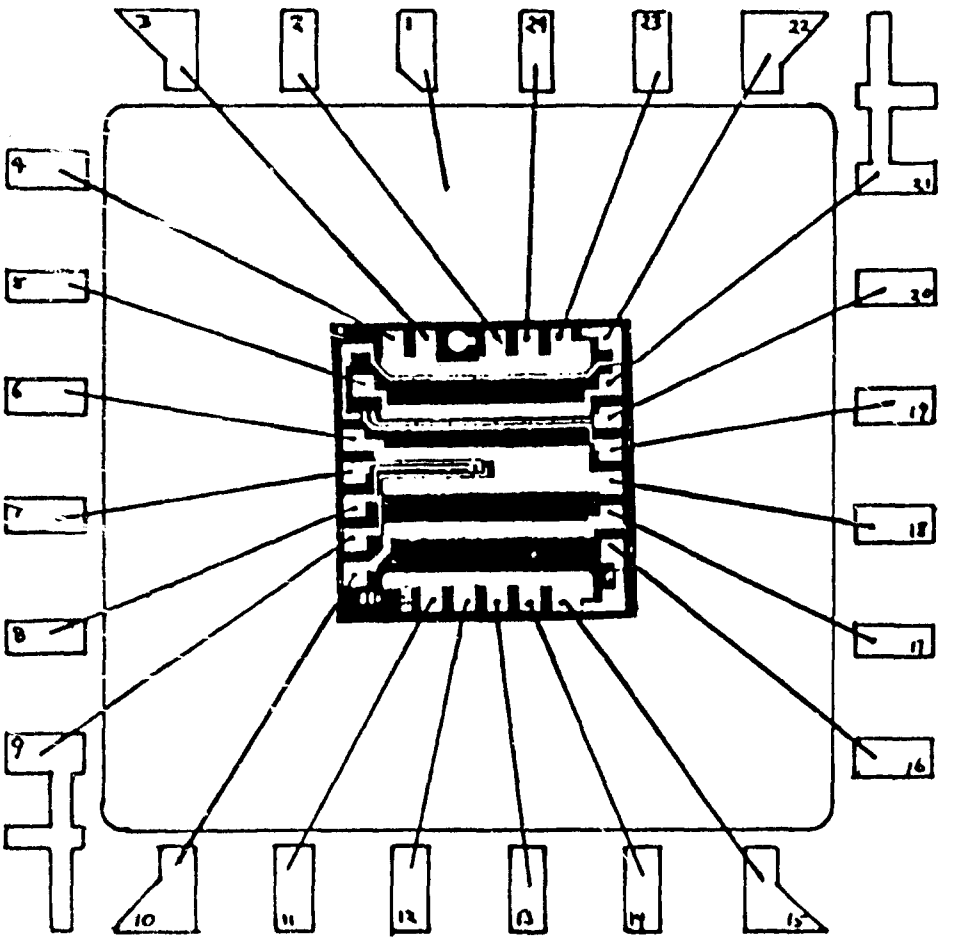
List of Packages
(continued)

Manufacturer	Part Number Identification	Case Outline Configuration
TRW	C2	C - 5
	C1 (.4 x .4)	C - 7
	C1 (.3 x .3)	C - 7
Zilog	71C0196-01	C - 5
	71C0101-01	D - 5 (3)
	71C0102-01	D - 5 (3)

HIGH TECHNOLOGY SENSORS, INC.
[illegible]

APPENDIX B

BONDING DIAGRAM



HIGH TECHNOLOGY SENSORS, INC.

Return Samples and Traveler To:
R. M. Mindock

TRAVELER
THERMAL RESISTANCE
MEASUREMENT
SAMPLE PREPARATION
CONTRACT NO. F30602-84-C-0067

Supplier Information

Supplier _____
Package Identification _____
Base _____
Lid _____
Lead Frame _____

Supplier Liason _____

Test Cell No. _____

Sample Construction Identification

Use the space below to identify how these test samples were prepared.

Use this space and the notes column to identify how the preparation of these samples differs from your certified product.

Back Preparation Sintered Au
Die Attachment Preform Size _____
Die Attachment Preform Thickness _____
Die Attachment Material Composition _____
Die Attachment Temperature _____
Bond Wire Size _____
Bond Wire Composition _____

Sample Preparation Process Steps

Step No.	Description	Quantity In	Quantity Out	Operator Initials	Notes
1.	Die Attachment	14			
2.	Wire Bond (See Attached Diagram) In cases wire bond length may exceed your design rules. Do not wire pull.				Bond per HTS Configuration Code _____
3.	Preseal Visual Reject units for improper fillet, cross wires to avoid shorts.				
4.	Seal				
5.	Leak check - Fine				
6.	Leak check - Gross				
7.	Identify Mark samples or bag and tag with test cell number and company name or logo. Identify rejects separately.				
8.	Return All Samples and Traveler To: Mr. R. M. Mindock High Technology Sensors 262 East Hornbeam Drive Longwood, Florida 32779 (305) 862-8182				

Revised 12/11/84

Test Lot No._____
Test Cell No._____

APPENDIX C

Test Procedure

Step	Description	Date	Operator
1.	Verify that hardware to be tested has appropriate test cell designation by consulting Appendix I of test plan.		
2.	Obtain test lot number by recording test cell number and date in test log. Obtain test traveler and data sheet and fill out test lot number and test cell number on data sheet and traveler.		
3.	Solder test leads to device.		
4.	Verify with volt/ohmeter that heater and sensing junction are bonded to appropriate leads per bonding diagram for test cell.		
5.	Verify that equipment is set up per test plan.		
6.	Determine that equipment to be used for measurement is within calibration.		
7.	Verify that ice bath and all electronics have been turned on and allowed to stabilize per manufacturers recommendation.		
8.	Load devices to adapter plate and attach leads. (Remove thermal grease from T/C hole and apply thermal grease to package prior to loading.) Record adapter plate number.		
9.	Verify continuity of devices by checking junction voltage with 1ma and heater voltage with 5 ma. Record continuity data.		
10.	Load adapter plate with devices into oven on liquid stabilized base. Attach washer thermocouple at one of the adapter plate fastening holes. Attach enclosure.		

Comments/Notes:

APPENDIX C
Test Procedure

Test Lot No._____
Test Cell No._____

Step	Description	Date	Operator
11.	Recheck continuity data.		
12.	Verify that device test thermocouple is making contact.		
13.	Set liquid stabilized bath for 100°C ±2°C. Record set point.		
14.	Set oven for 100°C ±2°C. Record room temperature.		
15.	Allow devices to stabilize with no power applied to the test device.		
16.	Record and record initial data on inlet thermocouple, outlet thermocouple adapter plate thermocouples and device thermocouples.		
17.	Verify stabilization per the following criteria. a). The device thermocouple shall be within ±5uV of established standard. b). The air temperature thermocouple shall be within 10uV of established standard. c). The inlet and outlet and adapter plate thermocouple shall be within ±7uV of established standard. d). The inlet and outlet thermocouple output shall not vary by more than ±5uV over a five minute period. e). The adapter plate thermocouple output shall not vary by more than ±5uV over a five minute period. f). The thermocouple reading for one device under test shall not vary by more than ±5uV over a five minute period.		

Comments/Notes:

APPENDIX C

Test Procedure

Test Lot No._____
Test Cell No._____

Step	Description	Date	Operator
18.	This space intentionally left blank.		
19.	Adjust current to the center junction (edge junction if appropriate) to 1.00± .001 ma for the device to be measured.		
20.	Measure and record forward voltage of the center junction device under test and the base thermocouple output.		
20.	Repeat for remaining devices.		
21.	Repeat for the first device measured. The forward voltage of the measuring junction shall agree within ±.00004 volt of the initial measurement. If not, repeat measurements for all devices.		
22.	Set oven and liquid bath to stabilize oven and adapter block at 80°C. Record water bath set point.		
23.	Verify stability at 80°C per the criteria of step 17. Record data.		
24.	Set heater current with potentiometers such that the forward voltage of the center junction of a device agrees within ±.00004 volts of reading obtained at 100°C.		
25.	Allow to stabilize.		

Comments/Notes:

Revised 12/11/84

Test Lot No._____
Test Cell No._____

APPENDIX C

Test Procedure

Step	Description	Date	Operator
26.	Verify that forward voltage readings are within ±.00004 volt of the average of the values obtained at 100°C, if not, repeat stabilization until agreement is obtained.		
27.	Read and record for each device the base thermocouple output, thermal chip forward voltage, heater voltage and heater current calculate θ_{jc}.		
28.	Repeat θ_{jc} measurements on first device. The thermal resistance calculated from the measurement must agree within ± 1% of the initial reading, if not, repeat the measurements on all units.		
29.	Calculate mean ($\bar{x}$) and standard deviation (σ) for the test cell.		
30.	If $2\sigma/\bar{x}$ is less than .15 remove all samples from test and store in appropriate location.		
31.	If $2\sigma/\bar{x}$ is greater than .15 repeat measurements on all units whose θ_{jc} values are greater than 1σ from the mean. If the θ_{jc} calculated from measurements on those devices repeat within 1% of initial reading, remove all samples from test and store in appropriate location. If not, repeat steps on all units until repeatability is obtained.		
32.	Input test data into computer for analysis.		

Comments/Notes:

Page 1 of 2

REVISED 12/11/84

ROOM TEMPERATURE _____

APPENDIX C

THERMAL RESISTANCE
DATA SHEET

TEST LOT NO._____

TEST CELL NO._____

ADAPTER PLATE NO._____

Continuity Check

Position	Device Serial No.	Junction Voltage at 1 ma (V)	Heater Current at 5ma (V)		Comment

Calibration

Position	Device Serial No.	Center Junction				Thermocouple			
		80°C	100°C			80°C	100°C		Comment

Thermal Measurements

Operator_____

Date _____

θ_{JC} Mean_____

θ_{JC} σ _____

2 $\sigma/\bar{x}$ _____

Position	Device Serial No	Base T/C		Chip Vc	Power		θ_{JC}
		MV			V	A	

Comments/Notes:

PAGE 2 of 2
REVISED 12-25-64
TEST LOT NO.
LOCATION

TEST POSITION

T/C POSITION		1	2	3	4	5	6 (INLET)	7 (OUTLET)	8 (AIR)	9 (STANDARD AIR)	10 (ENCLOSURE TOP)	11 (BATH)	12 (BLOCK)	OVEN
T/C No.		18	7	9	14	15	10	4	12	2	11	3	17	
BATH SET POINT	TIME													
100°C min		4.285	4.285	4.286	4.287	4.288	4.284	4.284		4.289			4.289	
100°C max		4.295	4.295	4.296	4.297	4.298	4.298	4.298		4.303			4.303	
80°C min		3.365	3.365	3.366	3.368	3.369	3.364	3.364		3.368			3.368	
80°C max		3.375	3.375	3.376	3.378	3.379	3.378	3.378		3.382			3.382	

APPENDIX D

The following pages contain data on individual test cells for the data groups. Each test cell contained a minimum of six devices. The following statistics are provided.

Abbreviation	Definition
Mean	Mean Value For Test Cell (°C/watt)
Median	Median Value For Test Cell (°C/watt)
Std. Dev. (SD)	Standard Deviation For Test Cell (°C/watt)
2SD/Mean	2 * Standard Deviation/Mean
MM	Median Moment as Defined in Report (°C/watt)
UMM	Upper Median Moment as Defined in Report (°C/watt)
LMM	Lower Median Moment as Defined in Report (°C/watt)
MM/SD	Median Moment/Standard Deviation
U/L	Upper Median Moment/Lower Median Moment

APPENDIX D-1

GROUP I - TEST CELL DATA

8 Lead Metal Can

MEAN	MED-IAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MN/ SD	U/L
57.39	57.81	1.309	.05	1.376	.867	1.915	1.05	.45
61.16	60.67	1.163	.04	1.262	1.679	.606	1.09	2.77
62.83	63.13	2.385	.08	2.404	2.412	2.589	1.01	.93
65.47	65.36	2.102	.06	2.105	2.113	2.098	1.00	1.01
65.69	65.69	2.124	.06	2.133	1.814	2.411	1.00	.75
66.03	66.16	2.272	.07	2.275	1.934	2.735	1.00	.71
67.05	66.56	2.396	.07	2.446	3.089	1.558	1.02	1.98

APPENDIX D-2

GROUP II - TEST CELL DATA
10 Lead Metal Can

MEAN	MED-IAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MM/ SD	U/L
55.78	55.51	1.603	.06	1.626	2.065	1.246	1.01	1.66
56.15	56.72	2.104	.07	2.179	1.535	2.673	1.04	.57
56.93	55.23	5.057	.18	5.335	7.801	.894	1.05	8.73
58.39	58.78	1.996	.07	2.033	1.528	2.574	1.02	.59
61.64	61.43	2.197	.07	2.207	2.452	1.932	1.00	1.27
62.10	61.50	2.092	.07	2.177	2.667	1.777	1.04	1.50

APPENDIX D-3

GROUP III - TEST CELL DATA

Chip Carriers (20-68 Terminal)

MEAN	MED-IAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MM/ SD	U/L
16.54	16.48	.504	.06	.507	.566	.439	1.01	1.29
16.86	17.01	.535	.06	.557	.366	.697	1.04	.52
17.37	17.44	.714	.08	.717	.727	.707	1.00	1.03
17.69	17.77	.577	.07	.583	.456	.735	1.01	.62
17.92	17.84	1.719	.19	1.721	1.829	1.605	1.00	1.14

APPENDIX D-4

GROUP IV - TEST CELL DATA

Glass Sealed Dual Inlines With 20 or Less Leads

MEAN	MED-IAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MM/ SD	U/L
17.21	17.18	.357	.04	.359	.437	.314	1.00	1.39
17.45	17.40	.547	.06	.549	.644	.434	1.00	1.49
17.75	17.80	.266	.03	.271	.203	.325	1.02	.63
18.16	18.53	1.018	.11	1.084	.610	1.474	1.07	.41
18.35	18.33	.336	.04	.336	.358	.348	1.00	1.03
18.46	18.23	.582	.06	.626	.863	.321	1.08	2.69
18.51	18.43	.626	.07	.631	.790	.501	1.01	1.58
18.70	18.67	.596	.06	.597	.684	.551	1.00	1.24
18.88	18.89	.628	.07	.628	.667	.587	1.00	1.13
19.42	19.32	1.162	.12	1.167	1.273	1.049	1.00	1.21
19.84	19.66	.580	.06	.608	.764	.394	1.05	1.94
19.92	19.82	.624	.06	.632	.827	.339	1.01	2.44
20.20	20.08	.731	.07	.741	.932	.567	1.01	1.64
20.50	20.58	.731	.07	.735	.654	.863	1.01	.76
20.75	20.69	.596	.06	.599	.678	.574	1.01	1.18
20.80	20.59	.885	.09	.910	1.148	.690	1.03	1.66
20.93	20.86	.766	.07	.769	.891	.625	1.00	1.42

APPENDIX D-4 (a)
GROUP IV - TEST CELL DATA
(continued)

MEAN	MED-IAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MM/ SD	U/L
21.19	20.97	.636	.06	.674	.881	.363	1.06	2.42
21.31	21.04	.770	.07	.815	1.101	.339	1.06	3.25
21.51	21.66	.899	.08	.913	.481	1.282	1.01	.37
21.65	21.58	.693	.06	.697	.799	.578	1.01	1.38
21.74	21.83	.770	.07	.775	.733	.875	1.01	.84
21.77	21.80	.703	.06	.703	.683	.779	1.00	.88
22.15	21.93	.495	.04	.542	.724	.253	1.10	2.87
22.29	22.10	.573	.05	.605	.845	.282	1.06	2.99
22.33	22.12	1.007	.09	1.029	1.303	.773	1.02	1.68
22.37	22.19	1.310	.12	1.322	1.669	.842	1.01	1.98
22.50	22.00	1.463	.13	1.545	2.216	.507	1.06	4.37
22.57	22.52	.758	.07	.760	.847	.661	1.00	1.28
22.63	22.83	.751	.07	.776	.475	.990	1.03	.48
22.68	22.32	1.226	.11	1.278	1.692	.633	1.04	2.67
22.71	21.46	2.660	.23	2.939	4.299	.486	1.11	8.84
22.79	22.87	.548	.05	.554	.475	.622	1.01	.76
22.89	22.39	1.508	.13	1.590	2.176	.566	1.05	3.85
22.96	22.07	2.344	.20	2.506	3.678	1.062	1.07	3.46

APPENDIX D-4 (a)
GROUP IV - TEST CELL DATA
(continued)

MEAN	MED-IAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MM/ SD	U/L
23.05	23.26	1.194	.10	1.213	.994	1.398	1.02	.71
23.11	23.11	.784	.07	.784	.891	.659	1.00	1.35
23.11	23.11	.784	.07	.784	.891	.659	1.00	1.35
23.50	23.59	1.612	.14	1.614	1.673	1.713	1.00	.98
23.56	23.34	1.428	.12	1.444	1.866	.830	1.01	2.25
23.57	22.96	2.732	.23	2.800	3.725	1.345	1.03	2.77
23.68	23.02	1.733	.15	1.854	2.501	.788	1.07	3.17
23.84	23.76	1.466	.12	1.468	1.612	1.307	1.00	1.23
24.20	24.32	1.101	.09	1.108	.916	1.271	1.01	.72
24.34	23.91	1.397	.11	1.461	2.060	.674	1.05	3.05
24.80	24.19	3.371	.27	3.426	4.328	2.179	1.02	1.99
24.89	23.53	3.540	.28	3.791	5.522	1.356	1.07	4.07
25.19	23.06	4.487	.36	4.965	7.318	.833	1.11	8.79
25.71	23.61	4.892	.38	5.326	7.469	.976	1.09	7.65
28.43	27.19	4.990	.35	5.142	6.873	3.802	1.03	1.81

APPENDIX D-5

GROUP V - TEST CELL DATA

Glass Sealed Dual Inlines With 22 or More Leads

MEAN	MED-IAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MM/ SD	U/L
18.09	18.09	.604	.07	.604	.700	.575	1.00	1.22
19.34	19.17	.707	.07	.729	.973	.340	1.03	2.86
19.58	19.57	.408	.04	.409	.439	.376	1.00	1.17
19.78	19.95	.909	.09	.925	.751	1.136	1.02	.66
20.57	20.62	1.211	.12	1.212	1.122	1.295	1.00	.87
20.73	20.20	1.934	.19	2.005	2.913	.595	1.04	4.90
21.87	21.20	2.426	.22	2.518	3.529	.475	1.04	7.43
22.02	21.85	1.064	.10	1.077	1.295	.936	1.01	1.38
22.35	22.09	.945	.08	.980	1.341	.561	1.04	2.39
22.52	22.16	1.201	.11	1.253	1.695	.728	1.04	2.33
23.93	23.65	1.874	.16	1.895	2.462	1.421	1.01	1.73
24.36	23.68	2.169	.18	2.273	3.381	.790	1.05	4.28

APPENDIX D-6

GROUP VI - TEST CELL DATA

Side Brazed Dual Inlines With 20 or Less Leads

MEAN	MED-IAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MM/ SD	U/L
14.95	14.80	.626	.08	.642	.808	.414	1.03	1.95
15.43	15.09	1.251	.16	1.297	1.700	.688	1.04	2.47
15.64	15.78	.748	.10	.760	.597	.893	1.02	.67
16.03	15.93	.569	.07	.578	.681	.523	1.02	1.30
16.52	16.41	.576	.07	.587	.718	.415	1.02	1.73
16.85	15.89	2.177	.26	2.383	3.276	.791	1.09	4.14
17.59	17.70	1.126	.13	1.131	.928	1.398	1.01	.66
17.93	17.53	.919	.10	1.000	1.375	.332	1.09	4.14
18.85	18.88	.685	.07	.686	.585	.823	1.00	.71
19.05	18.59	1.445	.15	1.517	2.034	.922	1.05	2.21
19.30	19.25	1.162	.12	1.163	1.222	1.101	1.00	1.11
19.33	19.25	1.494	.15	1.497	1.665	1.307	1.00	1.27
21.08	21.39	1.674	.16	1.703	1.464	2.150	1.02	.68

APPENDIX D-7

GROUP VII - TEST CELL DATA

Side Brazed Dual Inlines With 22 or More Leads

MEAN	MED-IAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MM/ SD	U/L
13.77	13.88	.494	.07	.506	.423	.620	1.02	.68
16.06	15.99	.505	.06	.510	.613	.381	1.01	1.61
17.08	16.94	.616	.07	.632	.766	.540	1.03	1.42
17.24	16.86	2.167	.25	2.200	2.936	1.027	1.01	2.86
18.94	18.96	.928	.10	.928	.942	.989	1.00	.95

APPENDIX D-8

GROUP VIII - TEST CELL DATA

Glass Sealed Flat Packages

MEAN	MEDIAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MM/ SD	U/L
14.63	14.45	.951	.13	.970	1.157	.735	1.02	1.57
15.76	16.00	1.140	.14	1.165	.933	1.358	1.02	.69
16.11	16.33	.901	.11	.927	.646	1.141	1.03	.57
16.39	15.94	1.599	.20	1.663	2.131	.996	1.04	2.14
16.69	16.35	1.876	.22	1.907	2.612	1.028	1.02	2.54
16.87	17.03	1.335	.16	1.344	1.343	1.504	1.01	.89
17.20	17.22	1.288	.15	1.289	1.321	1.255	1.00	1.05
18.51	17.54	3.198	.35	3.344	4.208	2.158	1.05	1.95
18.68	18.74	1.013	.11	1.015	.927	1.096	1.00	.85
18.86	18.67	1.308	.14	1.322	1.600	.968	1.01	1.65
18.94	18.56	.864	.09	.946	1.305	.297	1.09	4.39
19.05	18.51	1.166	.12	1.286	1.738	.536	1.10	3.24
20.02	20.43	1.652	.17	1.702	1.275	2.180	1.03	.58

APPENDIX D-9

GROUP IX - TEST CELL DATA

Bottom Braze Flat Packages

MEAN	MED-IAN	STD DEV (SD)	2SD/ MEAN	MM	UMM	LMM	MM/ SD	U/L
13.66	13.53	.554	.08	.570	.719	.363	1.03	1.98
13.80	13.92	.443	.06	.459	.350	.592	1.03	.59
15.22	15.01	.980	.13	1.002	1.257	.654	1.02	1.92
16.63	16.41	.964	.12	.989	1.230	.667	1.03	1.84
17.73	17.45	.964	.11	1.005	1.311	.709	1.04	1.85
18.42	18.37	1.028	.11	1.030	1.235	.928	1.00	1.33
18.54	17.51	2.510	.27	2.714	3.776	.690	1.08	5.47
18.99	19.22	.917	.10	.945	.634	1.177	1.03	.54

IX. LIST OF ABBREVIATIONS AND SYMBOLS

A_c	Chip Area
cal	Calories
cm	Centimeter
DIP	Dual Inline Package
DoD	Department of Defense
LMM	Lower Median Moment
LSI	Large Scale Integration
M_d	Median Thermal Resistance
MM	Median Moment
MSI	Medium Scale Integration
N	Number of Samples
N_L	Number of Samples Less Than the Median
N_U	Number of Samples Greater Than the Median
SD	Standard Deviation
sec	Second
SSI	Small Scale Integration
t	t Statistic
T_c	Case Temperature
θ_{jc}	Thermal Resistance From Junction To Case
T.I.	Texas Instruments
U/L	Upper Median Moment/Lower Median Moment
UMM	Upper Median Moment
V_{BE}	Emitter Base Junction Forward Voltage

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